Fault Protection, 6 Ω R_{ON}, SPST Switch with 0.6 kΩ Feedback Channel

Data Sheet **ADG5401F**

FEATURES

- Analog output protection and detection solution
  - Overvoltage protection up to ±60 V on S and SFB pins
  - Power off protection up to ±60 V on S and SFB pins
  - Integrated 0.6 kΩ secondary feedback channel
- Known output under all conditions
  - User enabled, power-on condition pulls source to 0 V
  - Known state without digital inputs present
- Optimized resistance for measurement channel and feedback channel
  - Low on resistance of 6 Ω typical on signal channel
  - Ultraflat, on resistance on signal channel
- Latch-up immune
- 3 mm × 2 mm LFCSP
- V_{SS} to V_{DD} −2 V signal range
  - Fully specified at ±15 V, ±20 V, +12 V, and +36 V
  - ±5 V to ±22 V dual-supply operation
  - 8 V to 44 V single-supply operation

APPLICATIONS

- DAC output protection
- Amplifier output protection
- Analog output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation

COMPANION PRODUCTS

- Current/Voltage Output DAC: AD5423
- Precision Amplifier: ADA4077-1
- Rail-to-Rail Output, JFET Op Amp: ADA4625-1

FUNCTIONAL BLOCK DIAGRAM

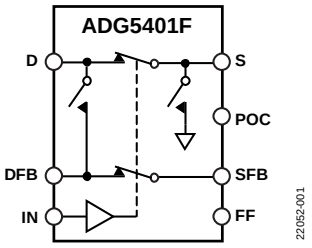

Figure 1.

GENERAL DESCRIPTION

The ADG5401F main channel switch is a SPST, low on-resistance switch that features overvoltage protection, power off protection, and overvoltage detection on the source pins (S and SFB). The ADG5401F also features a protected secondary feedback channel for use with digital-to-analog converter (DAC) or amplifier outputs.

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance.

When powered, if the analog input signal levels on the S pin exceed V_{DD} or V_{SS} by a threshold voltage (V_T) the switch turns off, the open-drain FF pin pulls to a logic low and a path between the D and DFB pins is switched on to prevent an open-loop condition on the amplifier output. Input signal levels up to +60 V or −60 V relative to ground are blocked, in both the powered and unpowered condition. The selectable POC pin function allows the protected switch terminal, S, to be connected to GND to minimize glitches on the output. The switch turns on with a Logic 1 input and conducts equally well in both directions. The digital input is compatible with 1.8 V logic inputs over the full operating supply range.

PRODUCT HIGHLIGHTS

1. Source pin is protected against voltages greater than the supply rails, up to −60 V and +60 V in both powered and unpowered states.
2. Overvoltage detection with digital output indicates operating state of switches.
3. Trench isolation guards against latch-up.
4. The ADG5401F can operate from a dual supply range of ±5 V to ±22 V or a single-supply range of +8 V to +44 V.
5. Negative channel metal oxide semiconductor (NMOS) only architecture requires 2 V headroom toward V_{DD} and provides low R_{ON} and ultraflat R_{ON} across the V_{SS} to V_{DD} − 5 V signal range.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

8/2020—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Operating Supply Voltages

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE				
Dual	±5		±22	V
Single	8		44	V

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 13.5 V, V_{SS} = −13.5 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
On Resistance, R_{ON}	6			Ω typ	Source voltage (V_S) = V_{SS} to 10 V, source current (I_S) = 10 mA
	8.5	10.5	12.5	Ω max	
	5.5			Ω typ	V_S = V_{SS} to 9 V, I_S = 10 mA
	7.5	9.5	11.5	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.35			Ω typ	V_S = V_{SS} to 10 V, I_S = 10 mA
	0.5	0.6	0.7	Ω max	
	0.02			Ω typ	V_S = V_{SS} to 9 V, I_S = 10 mA
	0.04	0.05	0.05	Ω max	
Feedback On Resistance, $R_{FEEDBACK}$	0.6			kΩ typ	V_S = V_{SS} to 10 V, I_S = −100 µA
	2.6	3.3	3.8	kΩ max	
LEAKAGE CURRENTS					V_{DD} = 16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±10 V, drain voltage (V_D) = ∓ 10 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓ 10 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = ±10 V, V_D = ±10 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C
Source Feedback Off Leakage, I_{SFB} (Off)	±0.1			nA typ	SFB voltage (V_{SFB}) = ±10 V, DFB voltage (V_{DFB}) = ∓ 10 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
Drain Feedback Off Leakage, I_{DFB} (Off)	±0.1			nA typ	V_{SFB} = ±10 V, V_{DFB} = ∓ 10 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
Channel On Feedback Leakage, I_{DFB} (On), I_{SFB} (On)	±0.1			nA typ	V_{SFB} = ±10 V, V_{DFB} = ±10 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
FAULT (ON S AND SFB PINS)					
V_T	0.7			V typ	
Source Leakage Current, I_S					
With Overvoltage			±55	µA typ	V_{DD} = 16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded or Floating			±11	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V
Drain Leakage Current, I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±60 V
	±0.3	±5	±55	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
	±0.3	±5	±55	nA max	
Power Supplies Floating			±2	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V
DIGITAL INPUTS/OUTPUTS					
Input Voltage High, V_{INH}			1.3	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Low or High Current, I_{INL} or I_{INH}	2.5			µA typ	Input voltage (V_{IN}) = 0 V or 5 V
			5	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
Output Voltage Low, V_{OL}	0.4			V max	Fault flag current (I_{FF}) = 2 mA
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	14.2			µs typ	Load resistance (R_L) = 300 Ω, load capacitance (C_L) = 35 pF, V_S = 10 V
	17	17.2	17.2	µs max	
Off Time, t_{OFF}	185			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
	220	220	220	ns max	
Overvoltage Response Time, $t_{RESPONSE}$					
Positive	230			ns typ	R_L = 1 kΩ, C_L = 5 pF
	230	240	240	ns max	
Negative	0.8			µs typ	R_L = 1 kΩ, C_L = 5 pF
	1	1.1	1.2	µs max	
Overvoltage Recovery Time, $t_{RECOVERY}$	11.7			µs typ	R_L = 1 kΩ, C_L = 5 pF
	14.4	14.5	14.5	µs max	
Interrupt Flag Response Time, $t_{DIGRESP}$	80			ns typ	Pull-up resistor (R_{PULLUP}) = 1 kΩ, C_L = 12 pF, pull-up voltage (V_{PULL_UP}) = 5 V
	90	95	100	ns max	
Interrupt Flag Recovery Time, t_{DIGREC}	1.5			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	2	2.2	2.2	µs max	
Charge Injection, Q_{INJ}	−230			pC typ	V_S = 0 V, source resistor (R_S) = 0 Ω, C_L = 1 nF

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency (f) = 1 MHz
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 10 V p-p, f = 20 Hz to 20 kHz
−3 dB Bandwidth	460			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Source Off Capacitance, C_S (Off)	9			pF typ	V_S = 0 V, f = 1 MHz
Drain Off Capacitance, C_D (Off)	11			pF typ	V_S = 0 V, f = 1 MHz
Drain On Capacitance and Source On Capacitance, C_D (On) and C_S (On)	19			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 16.5 V, V_{SS} = −16.5 V, GND = 0 V, digital inputs = 0 V or 5 V
Normal Mode					
Positive Supply Current, I_{DD}	165			µA typ	
	240		240	µA max	
GND Current, I_{GND}	85			µA typ	
	120		120	µA max	
Negative Supply Current, I_{SS}	80			µA typ	
	120		120	µA max	
Fault Mode (on S and SFB Pins)					V_S = ±60 V
I_{DD}	140			µA typ	
	230		230	µA max	
I_{GND}	100			µA typ	
	150		150	µA max	
I_{SS}	65			µA typ	
	110		110	µA max	

±20 V DUAL SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 18 V, V_{SS} = −18 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
R_{ON}	6			Ω typ	V_S = V_{SS} to 15 V, I_S = 10 mA
	8.5	10.5	12.5	Ω max	
	5.5			Ω typ	V_S = V_{SS} to 13.5 V, I_S = 10 mA
	7.5	9.5	11.5	Ω max	
$R_{FLAT (ON)}$	0.35			Ω typ	V_S = V_{SS} to 15 V, I_S = 10 mA
	0.5	0.6	0.7	Ω max	
	0.02			Ω typ	V_S = V_{SS} to 13.5 V, I_S = 10 mA
	0.04	0.05	0.05	Ω max	
$R_{FEEDBACK}$	0.6			kΩ typ	V_S = V_{SS} to 15 V, I_S = 100 µA
	2.6	3.3	3.8	kΩ max	
LEAKAGE CURRENTS					V_{DD} = 22 V, V_{SS} = −22 V
I_S (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓ 15 V
	±0.2	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓ 15 V
	±0.2	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_D (On), I_S (On)	±0.1			nA typ	V_S = ±15 V, V_D = ±15 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C
I_{SFB} (Off)	±0.1			nA typ	V_{SFB} = ±15 V, V_{DFB} = ∓ 15 V
	±0.2	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_{DFB} (Off)	±0.1			nA typ	V_{SFB} = ±15 V, V_{DFB} = ∓ 15 V
	±0.2	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_{DFB} (On), I_{SFB} (On)	±0.1			nA typ	V_{SFB} = ±15 V, V_{DFB} = ±15 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C
FAULT (ON S AND SFB PINS)					
V_T	0.7			V typ	
I_S					
With Overvoltage			±55	µA typ	V_{DD} = 22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±58 V
Power Supplies Grounded or Floating			±11	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±58 V
	±0.3	±5	±55	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
	±0.3	±5	±55	nA max	
Power Supplies Floating			±2	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V
DIGITAL INPUTS/OUTPUTS					
V_{INH}			1.3	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	2.5			µA typ	V_{IN} = 0 V or 5 V
			5	µA max	
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	15.9			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
	19.1	19.3	19.4	µs max	
t_{OFF}	180			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
	210	220	220	ns max	
$t_{RESPONSE}$					
Positive	230			ns typ	R_L = 1 kΩ, C_L = 5 pF
	230	230	230	ns max	
Negative	0.7			µs typ	R_L = 1 kΩ, C_L = 5 pF
	0.9	0.9	1	µs max	
$t_{RECOVERY}$	13.8			µs typ	R_L = 1 kΩ, C_L = 5 pF
	16.8	16.9	16.9	µs max	
$t_{DIGRESP}$	80			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	90	95	100	ns max	
t_{DIGREC}	1.9			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	2.4	2.6	2.6	µs max	
Q_{INJ}	−270			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 10 V p-p, f = 20 Hz to 20 kHz
−3 dB Bandwidth	450			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (Off)	8			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	10			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	18			pF typ	V_S = 0 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 22 V, V_{SS} = −22 V, GND = 0 V, digital inputs = 0 V or 5 V
Normal Mode					
I_{DD}	165			µA typ	
	240		240	µA max	
I_{GND}	85			µA typ	
	120		120	µA max	
I_{SS}	80			µA typ	
	120		120	µA max	
Fault Mode (on S and SFB Pins)					V_S = ±58 V
I_{DD}	140			µA typ	
	230		230	µA max	
I_{GND}	100			µA typ	
	150		150	µA max	
I_{SS}	65			µA typ	
	110		110	µA max	

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
R_{ON}	6			Ω typ	V_S = 0 V to 8 V, I_S = 10 mA
	8.5	10.5	12.5	Ω max	
	5.5			Ω typ	V_S = 0 V to 6 V, I_S = 10 mA
	7.5	9.5	11.5	Ω max	
$R_{FLAT (ON)}$	0.6			Ω typ	V_S = 0 V to 8 V, I_S = 10 mA
	0.8	0.9	1.0	Ω max	
	0.01			Ω typ	V_S = 0 V to 6 V, I_S = 10 mA
	0.04	0.05	0.05	Ω max	
$R_{FEEDBACK}$	0.6			kΩ typ	V_S = V_{SS} to 8 V, I_S = 100 µA
	2.7	3.4	3.9	kΩ max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
I_S (Off)	±0.1			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_D (Off)	±0.1			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_D (On), I_S (On)	±0.1			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C
I_{SFB} (Off)	±0.1			nA typ	V_{SFB} = 1 V to 10 V, V_{DFB} = 10 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_{DFB} (Off)	±0.1			nA typ	V_{SFB} = 1 V to 10 V, V_{DFB} = 10 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_{DFB} (On), I_{SFB} (On)	±0.1			nA typ	V_{SFB} = V_{DFB} = 1 V to 10 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C
FAULT (ON S AND SFB PINS)					
V_T	0.7			V typ	
I_S					
With Overvoltage			±55	µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded or Floating			±11	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
	±0.3	±5	±55	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
	±0.3	±5	±55	nA max	
Power Supplies Floating			±2	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V
DIGITAL INPUTS/OUTPUTS					
V_{INH}			1.3	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	2.5			µA typ	V_{IN} = 0 V or 5 V
			5	µA max	
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	6.5			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V
	7.6	7.6	7.6	µs max	
t_{OFF}	285			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V
	340	350	350	ns max	
$t_{RESPONSE}$					
Positive	320			ns typ	R_L = 1 kΩ, C_L = 5 pF
	320	330	330	ns max	
Negative	1.3			µs typ	R_{PULLUP} = 1 kΩ, C_L = 5 pF
	1.5	1.7	1.8	µs max	
$t_{RECOVERY}$	6.1			µs typ	R_L = 1 kΩ, C_L = 5 pF
	7.1	7.7	8	µs max	
$t_{DIGRESP}$	80			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	90	95	100	ns max	
t_{DIGREC}	1.3			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	1.7	1.9	1.9	µs max	
Q_{INJ}	−120			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
THD + N	0.0017			% typ	R_L = 10 kΩ, V_S = 6 V p-p, f = 20 Hz to 20 kHz
−3 dB Bandwidth	390			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1MHz
C_S (Off)	12			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	14			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	20			pF typ	V_S = 6 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, digital inputs = 0 V or 5 V
Normal Mode					
I_{DD}	150			µA typ	
	220		220	µA max	
I_{GND}	90			µA typ	
	130		130	µA max	
I_{SS}	60			µA typ	
	90		90	µA max	
Fault Mode (on S and SFB Pins)					V_S = ±60 V
I_{DD}	140			µA typ	
	230		230	µA max	
I_{GND}	100			µA typ	
	150		150	µA max	
I_{SS}	65			µA typ	
	110		110	µA max	

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 5.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 32.4 V, V_{SS} = 0 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
R_{ON}	6			Ω typ	V_S = 0 V to 30 V, I_S = 10 mA
	8.5	10.5	12.5	Ω max	
	5.5			Ω typ	V_S = 0 V to 27 V, I_S = 10 mA
	7.5	9.5	11.5	Ω max	
$R_{FLAT (ON)}$	0.6			Ω typ	V_S = 0 V to 30 V, I_S = 10 mA
	0.8	0.9	1.0	Ω max	
	0.01			Ω typ	V_S = 0 V to 27 V, I_S = 10 mA
	0.04	0.05	0.05	Ω max	
$R_{FEEDBACK}$	0.6			kΩ typ	V_S = 0 V to 30 V, I_S = 100 µA
	2.7	3.4	3.9	kΩ max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
I_S (Off)	±0.1			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_D (Off)	±0.1			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_D (On), I_S (On)	±0.1			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C
I_{SFB} (Off)	±0.1			nA typ	V_{SFB} = 1 V to 30 V, V_{DFB} = 30 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_{DFB} (Off)	±0.1			nA typ	V_{SFB} = 1 V to 30 V, V_{DFB} = 30 V to 1 V
	±0.15	±2.5	±35	nA max	
			±11.5	nA max	−40°C to +105°C
I_{DFB} (On), I_{SFB} (On)	±0.1			nA typ	V_{SFB} = V_{DFB} = 1 V to 30 V
	±0.3	±3	±40	nA max	
			±12	nA max	−40°C to +105°C
FAULT (ON S AND SFB PINS)					
V_T	0.7			V typ	
I_S					
With Overvoltage			±55	µA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +60 V and V_S = −40 V
Power Supplies Grounded or Floating			±11	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +60 V and V_S = −40 V
	±0.3	±5	±55	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
	±0.3	±5	±55	nA max	
Power Supplies Floating			±2	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V
DIGITAL INPUTS/OUTPUTS					
V_{INH}			1.3	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	2.5			µA typ	V_{IN} = 0 V or 5 V
			5	µA max	
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	8.7			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V
	10.2	10.3	10.3	µs max	
t_{OFF}	310			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V
	360	360	360	ns max	
$t_{RESPONSE}$					
Positive	330			ns typ	R_L = 1 kΩ, C_L = 5 pF
	350	350	350	ns max	
Negative	1.3			µs typ	R_{PULLUP} = 1 kΩ, C_L = 5 pF
	1.5	1.6	1.8	µs max	
$t_{RECOVERY}$	6.2			µs typ	R_L = 1 kΩ, C_L = 5 pF
	9.4	9.4	9.7	µs max	
$t_{DIGRESP}$	80			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	95	100	100	ns max	
t_{DIGREC}	3.3			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	6.1	6.3	6.6	µs max	
Q_{INJ}	−230			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
THD + N	0.0008			% typ	R_L = 10 kΩ, V_S = 18 V p-p, f = 20 Hz to 20 kHz
−3 dB Bandwidth	395			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (Off)	9			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	11			pF typ	V_S = 18 V, f = 1 MHz
CD (On), C_S (On)	18			pF typ	V_S = 18 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, digital inputs = 0 V or 5 V
Normal Mode					
I_{DD}	150			µA typ	
	220		220	µA max	
I_{GND}	90			µA typ	
	130		130	µA max	
I_{SS}	60			µA typ	
	90		90	µA max	
Fault Mode (on S and SFB Pins)					V_S = +60 V and V_S = −40 V
I_{DD}	140			µA typ	
	230		230	µA max	
I_{GND}	100			µA typ	
	150		150	µA max	
I_{SS}	65			µA typ	
	110		110	µA max	

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 6.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, S OR D					
θ_{JA} = 170°C/W	163	105	63	mA max	$V_S = V_{SS}$ to V_{DD} − 5 V
	151	99	61	mA max	$V_S = V_{SS}$ to V_{DD} − 2 V

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Value
V_{DD} to V_{SS}	60 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	−28 V to +0.3 V
S or SFB to GND	−60 V to +60 V
S or SFB to V_{DD}	80 V
S or SFB to V_{SS}	80 V
S to D	80 V
SFB to DFB	80 V
D or DFB[1]	V_{SS} − 0.7 V to V_{DD} + 0.7 V or 30 mA, whichever occurs first
Digital Inputs	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Peak Current, S or D Pin	515 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D Pin	Data + 15%[2]
Digital Output	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

[1] Overvoltages at the D and DFB pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 6.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-10-16	170	58.2	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADG5401F

Table 9. ADG5401F, 10-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM[1]	2	2

[1] This is the HBM for the input/output port to supplies, the input/output port to input/output port, and for all other pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

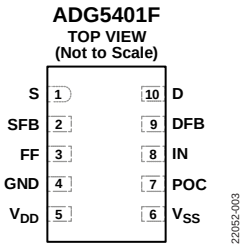

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S	Overvoltage Protected Source Terminal. The S pin can be an input or an output.
2	SFB	Overvoltage Protected Source Terminal of the Feedback Channel. The SFB pin can be an input or an output.
3	FF	Fault Flag Digital Output. The FF pin is an open-drain output that requires an external pull-up resistor. This digital output pulls low when a fault condition occurs on either the S or SFB input.
4	GND	Ground (0 V) Reference.
5	V_{DD}	Most Positive Power Supply Potential.
6	V_{SS}	Most Negative Power Supply Potential.
7	POC	Power-On Condition. The POC pin determines the power-on condition of the source pin (S).
8	IN	Logic Control Input.
9	DFB	Drain Terminal of the Feedback Channel. The DFB pin can be an input or an output.
10	D	Drain Terminal. The D pin can be an input or an output.

TYPICAL PERFORMANCE CHARACTERISTICS

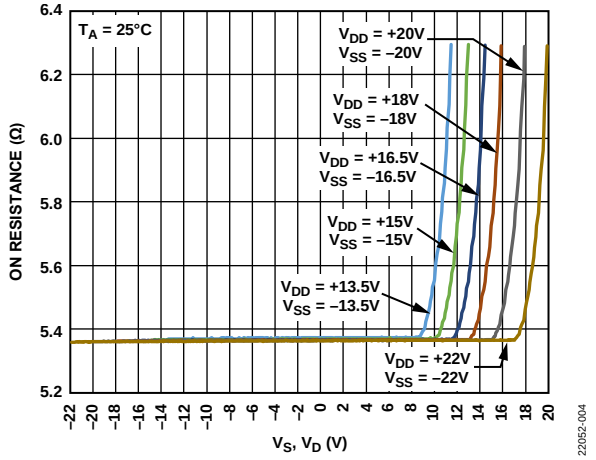

Figure 3. On Resistance as a Function of V_S,V_D (Dual Supply)

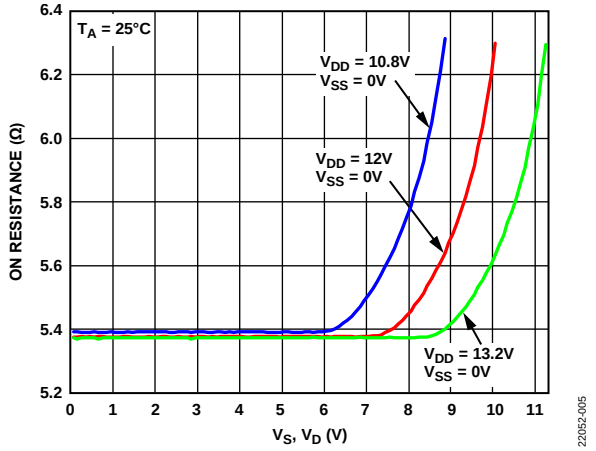

Figure 4. On Resistance as a Function of V_S,V_D (12 V Single Supply)

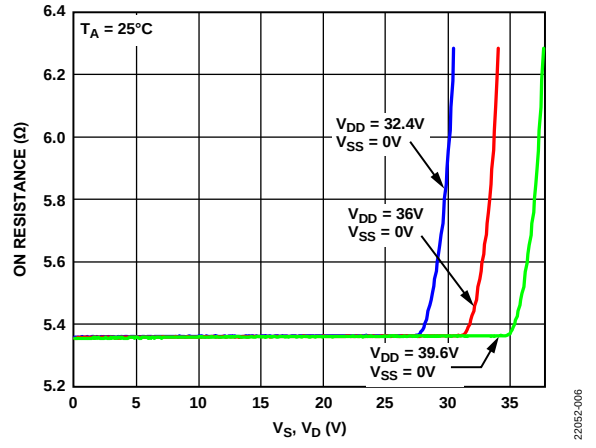

Figure 5. On Resistance as a Function of V_S,V_D (36 V Single Supply)

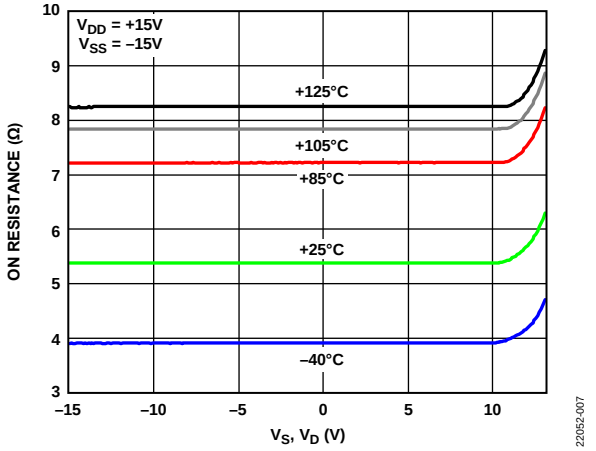

Figure 6. On Resistance as a Function of V_S,V_D for Different Temperatures, ±15 V Dual Supply

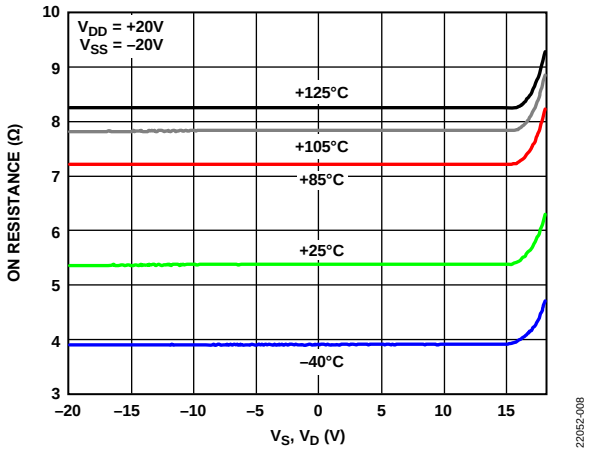

Figure 7. On Resistance as a Function of V_S,V_D for Different Temperatures, ±20 V Dual Supply

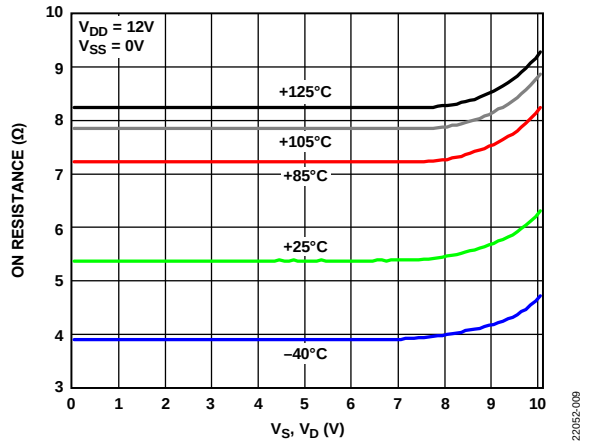

Figure 8. On Resistance as a Function of V_S,V_D for Different Temperatures, 12 V Single Supply

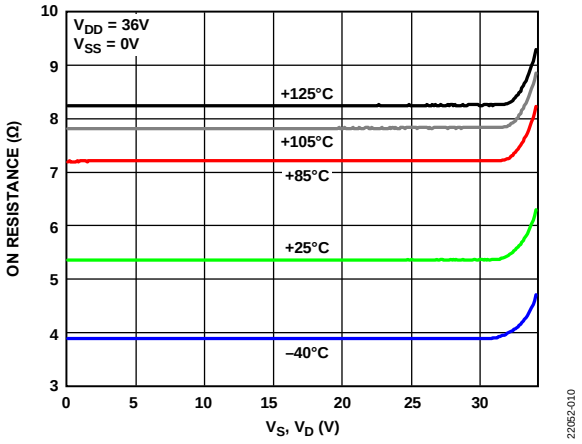

Figure 9. On Resistance as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

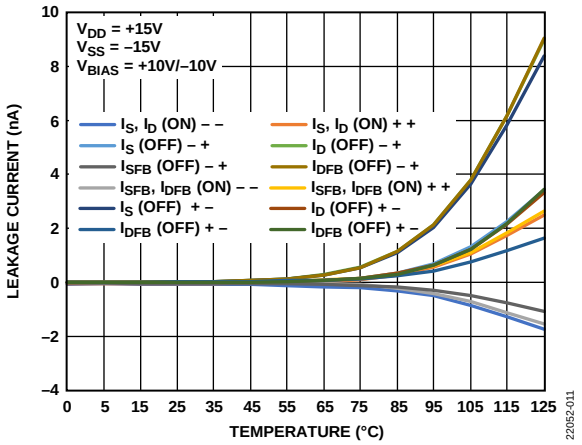

Figure 10. Leakage Current vs. Temperature, ±15 V Dual Supply (V_{BIAS} Is the Bias Voltage)

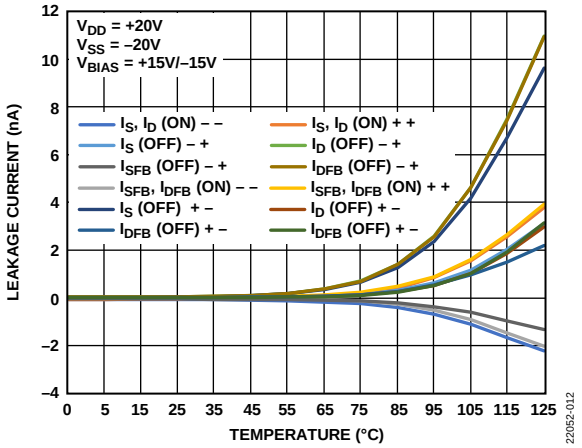

Figure 11. Leakage Current vs. Temperature, ±20 V Dual Supply

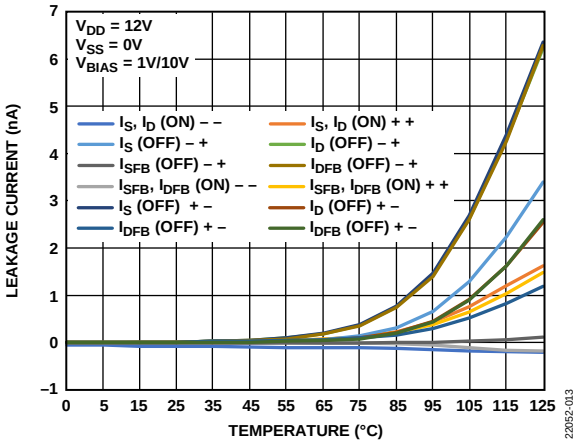

Figure 12. Leakage Current vs. Temperature, 12 V Single Supply

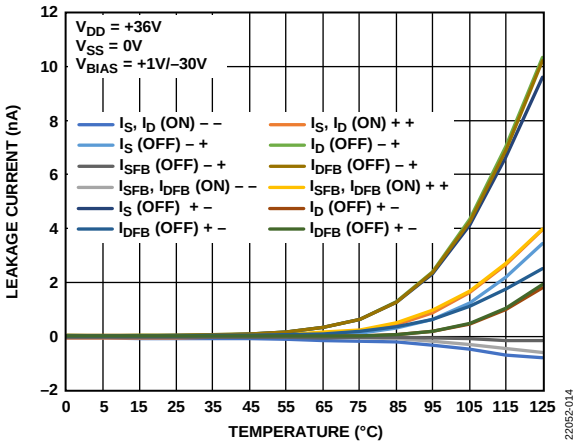

Figure 13. Leakage Current vs. Temperature, 36 V Single Supply

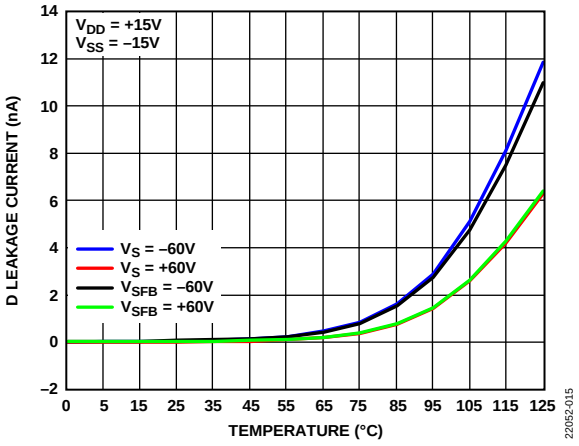

Figure 14. D Leakage Current vs. Temperature During Overvoltage, ±15 V Dual Supply

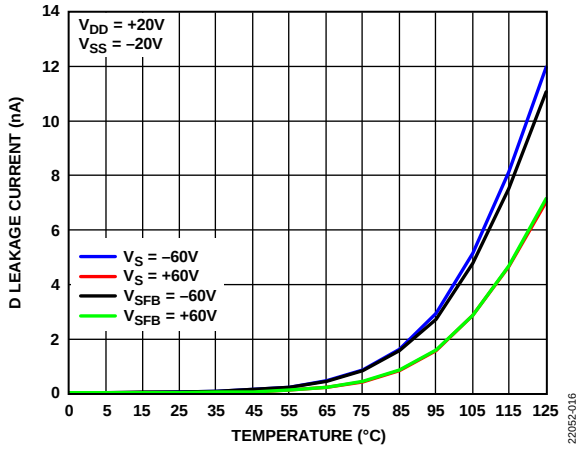

Figure 15. D Leakage Current vs. Temperature During Overvoltage, ±20 V Dual Supply

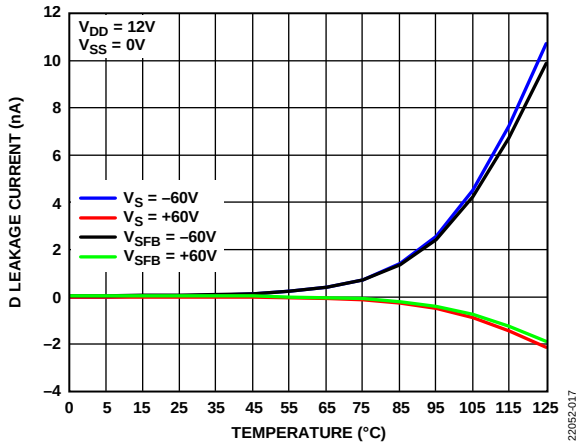

Figure 16. D Leakage Current vs. Temperature During Overvoltage, 12 V Single Supply

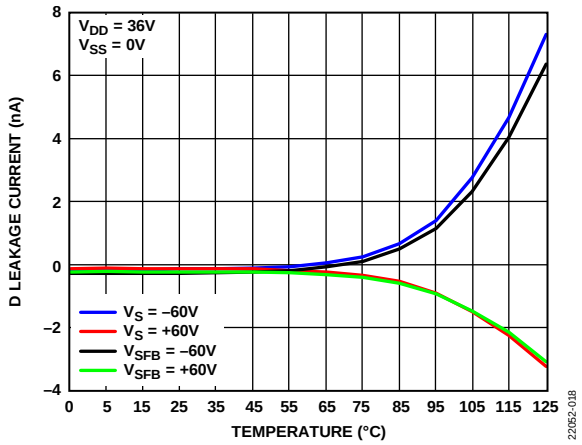

Figure 17. D Leakage Current vs. Temperature During Overvoltage, 36 V Single Supply

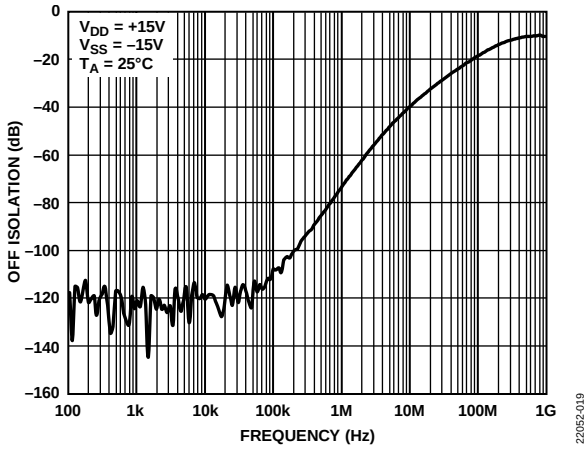

Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply

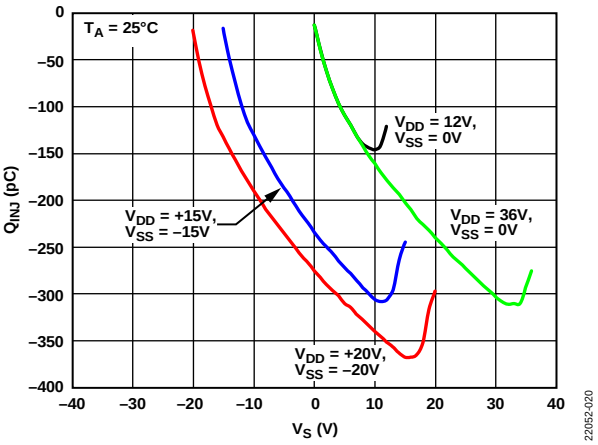

Figure 19. Q_{INJ} vs. V_S

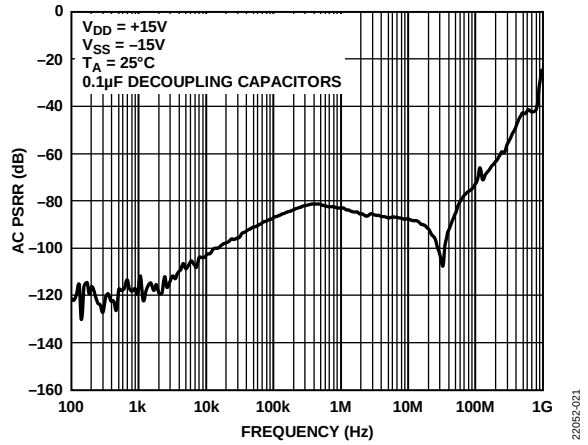

Figure 20. AC Power Supply Rejection Ratio (PSRR) vs. Frequency, ±15 V Dual Supply

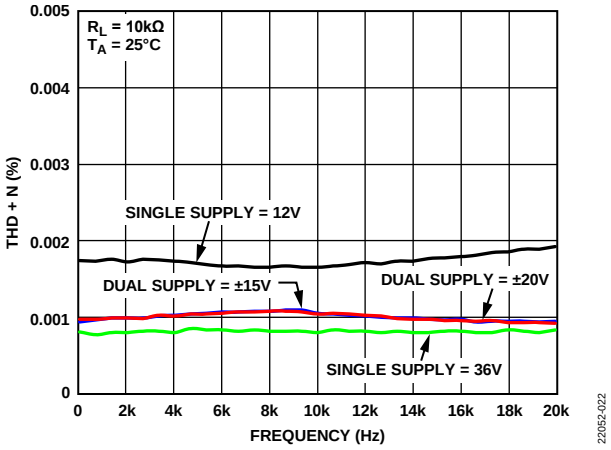

Figure 21. THD + N vs. Frequency

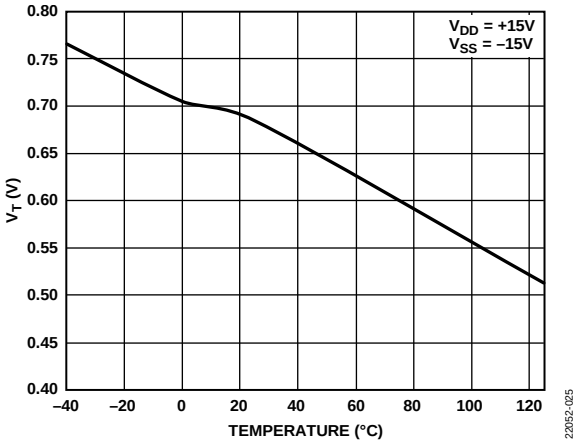

Figure 24. V_T vs. Temperature, ±15 V Dual Supply

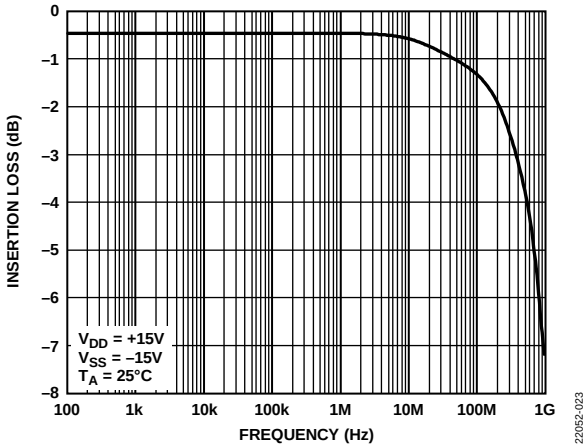

Figure 22. Insertion Loss vs. Frequency

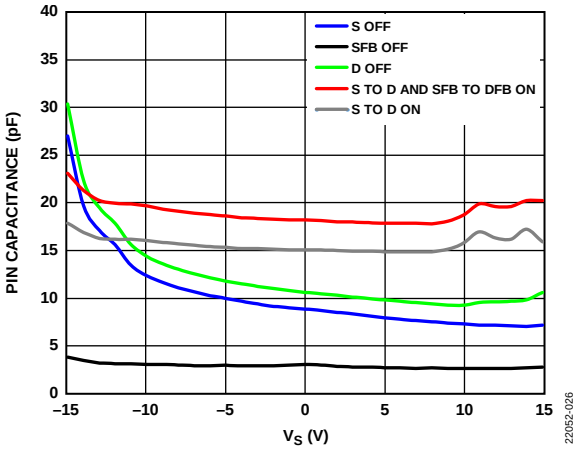

Figure 25. Pin Capacitance vs. V_S

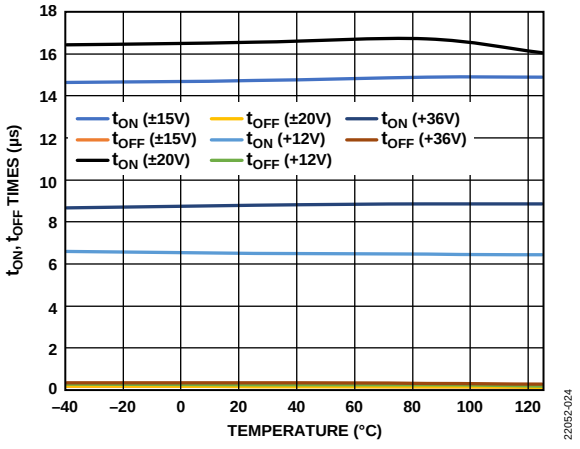

Figure 23. t_{ON}, t_{OFF} Times vs. Temperature for Various Supplies

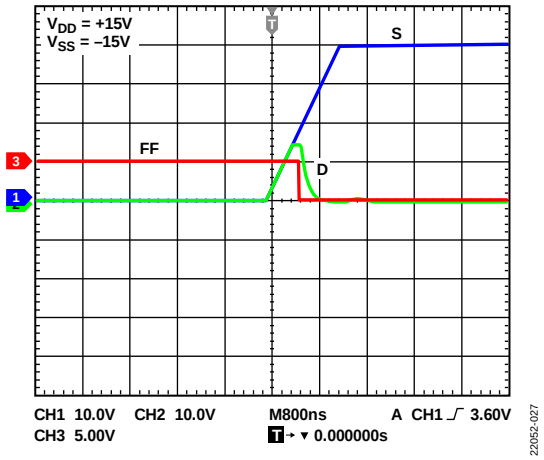

Figure 26. Drain Output Response to Positive Overvoltage

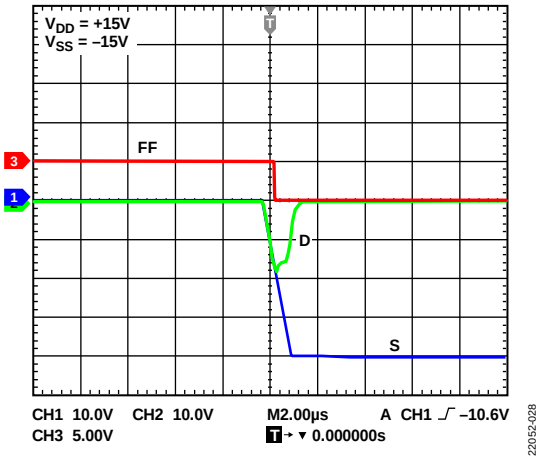

Figure 27. Drain Output Response to Negative Overvoltage

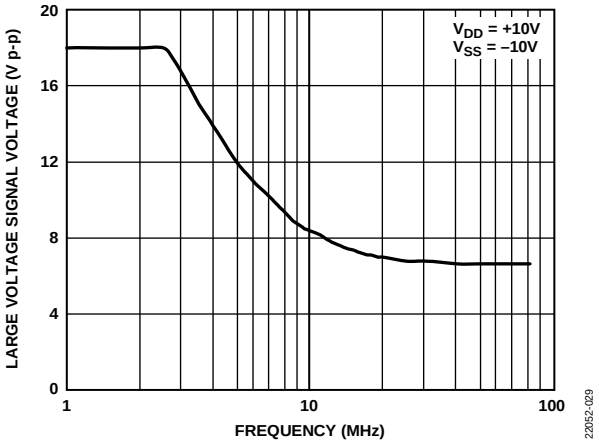

Figure 28. Large Voltage Signal Voltage vs. Frequency

TEST CIRCUITS

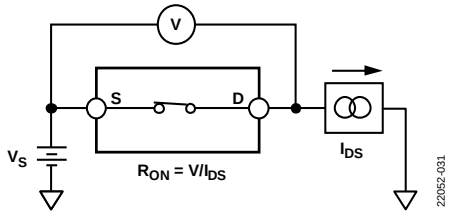

Figure 29. On Resistance (I_{DS} Is the Drain to Source Current.)

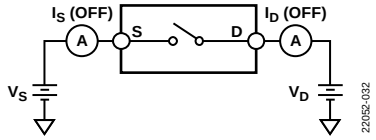

Figure 30. Off Leakage

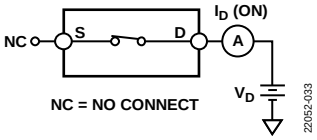

Figure 31. On Leakage

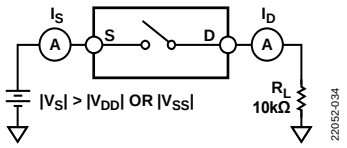

Figure 32. Switch Overvoltage Leakage

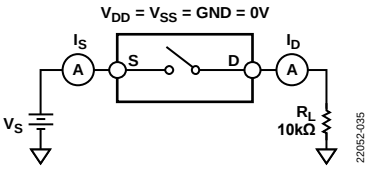

Figure 33. Switch Unpowered Leakage

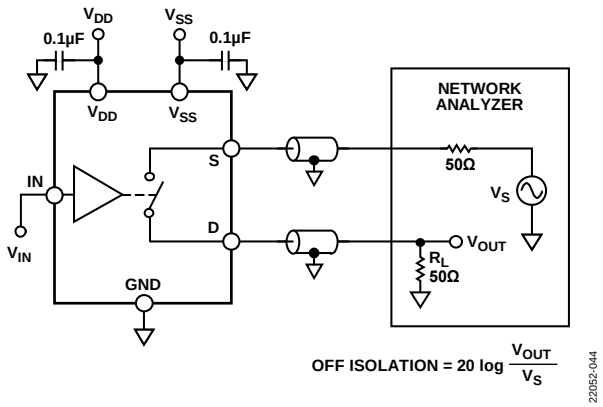

Figure 34. Off Isolation (V_{OUT} Is the Output Voltage)

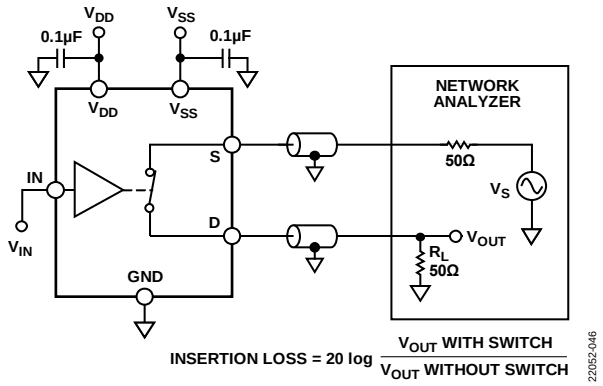

Figure 35. Bandwidth

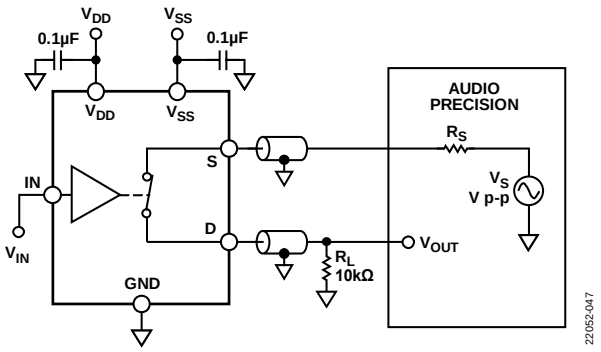

Figure 36. THD + N

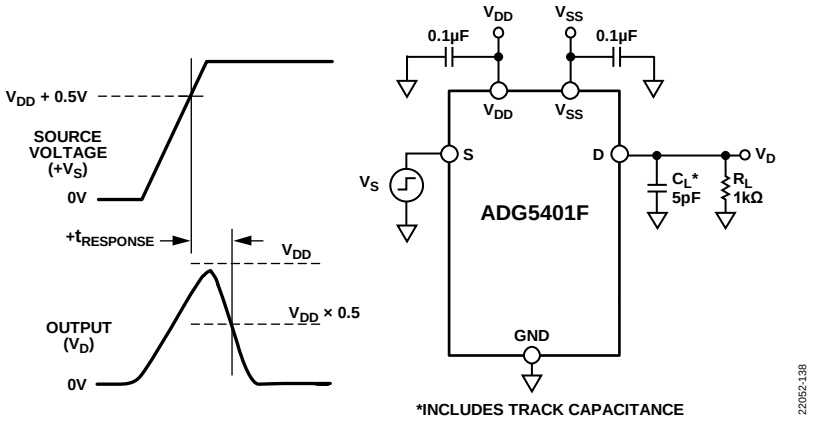

Figure 37. Overvoltage Response Time, $t_{RESPONSE}$

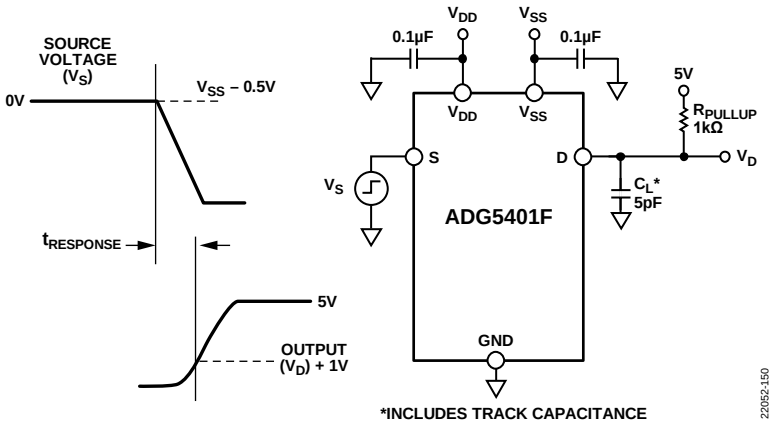

Figure 38. Negative Overvoltage Response Time, Single-Supply, $t_{RESPONSE}$

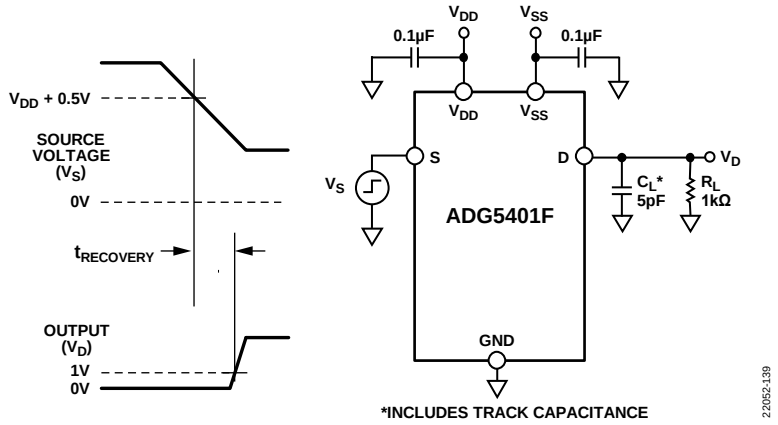

Figure 39. Overvoltage Recovery Time, $t_{RECOVERY}$

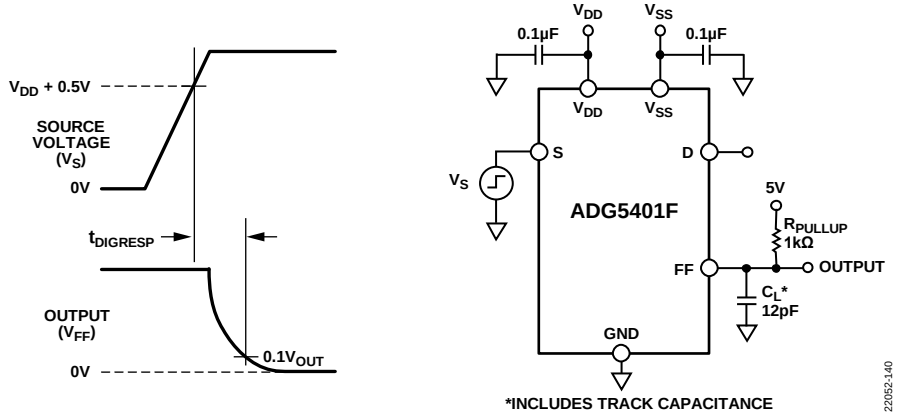

Figure 40. Interrupt Flag Response Time, $t_{DIGRESP}$ (V_{FF} Is the Fault Flag Voltage)

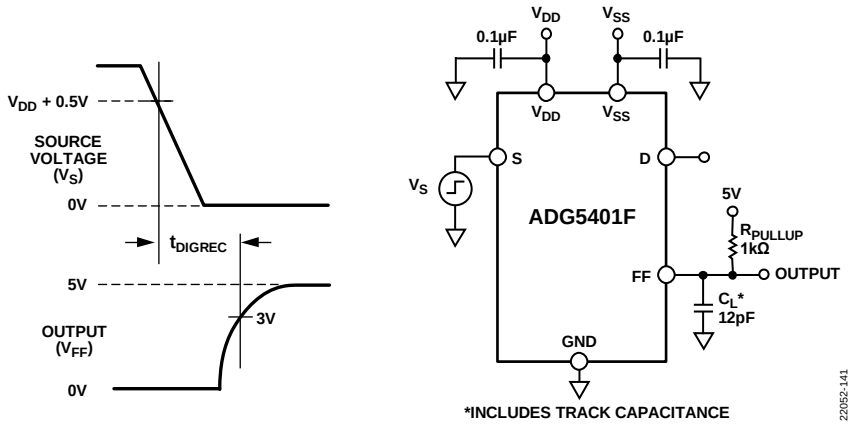

Figure 41. Interrupt Flag Recovery Time, t_{DIGREC}

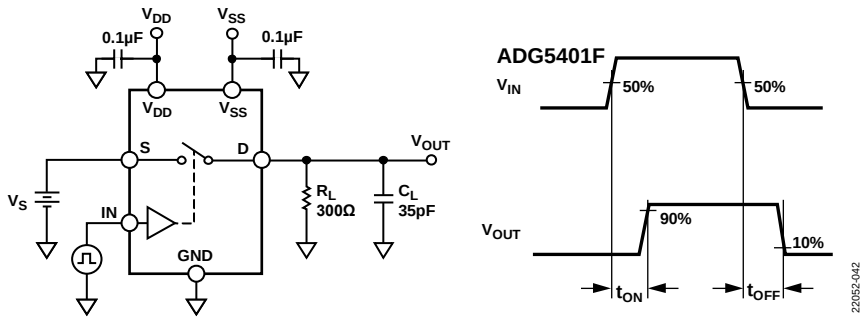

Figure 42. Switching Times, t_{ON} and t_{OFF}

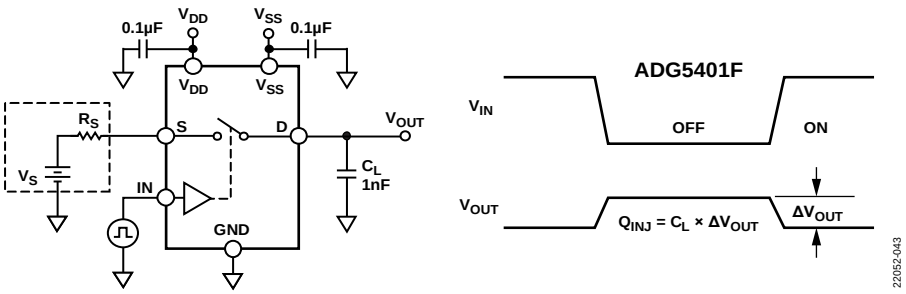

Figure 43. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on the D and DFB pins and the S and SFB pins, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between the D and DFB pins and the S and SFB pins.

$R_{FLAT (ON)}$
$R_{FLAT (ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch D pin capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch S pin capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on (see Figure 42).

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off (see Figure 42).

$t_{DIGRESP}$
$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to voltage on the source pin exceeding the supply voltage by 0.5 V.

t_{DIGREC}
t_{DIGREC} is the time required for the FF pin to return high, measured with respect to voltage on the S pin falling below the supply voltage plus 0.5 V.

$t_{RESPONSE}$
$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

$t_{RECOVERY}$
$t_{RECOVERY}$ represents the delay between an overvoltage on the S pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

−3 dB Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

THD + N
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)
AC PSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. AC PSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

V_T
V_T is the voltage threshold at which the overvoltage protection circuitry engages (see Figure 24).

THEORY OF OPERATION

SWITCH ARCHITECTURE

The ADG5401F consists of two switch channels of N channel diffused metal-oxide semiconductor (NDMOS) transistors, a main channel switch and a secondary feedback channel switch. This construction provides excellent R_{ON} performance in a small area. The ADG5401F main channel operates as a standard switch when input signals with a voltage between V_{SS} and V_{DD} − 2 V are applied. For example, the on resistance is 6 Ω typically, and the IN pin controls when the switch opens or closes. The secondary switch channel on resistance is 0.6 kΩ. The IN pin controls when both switches open or close.

Additional internal circuitry enables the switches to detect overvoltage inputs by comparing the voltage on both the S and SFB pins with the V_{DD} and V_{SS} pins. A signal is considered overvoltage when the signal exceeds the supply voltages by V_T. V_T is typically 0.7 V but can range from 0.76 V at −40°C down to 0.5 V at +125°C. See Figure 24 to see the change in V_T with the operating temperature.

When an overvoltage condition is detected on either the S or SFB pin, both switches automatically open regardless of the digital logic state (IN). The S to D and SFB to DFB pins become high impedance and ensure that no current flows through the switches. In Figure 26, the voltage on the D pin follows the voltage on the S pin until the main channel switch turns off completely and the drain voltage discharges through the load. The maximum voltage on the drain is limited by the internal ESD diodes, and the rate at which the output voltage discharges is dependent on the load at the D pin.

The maximum voltage that can be applied to any source input is +60 V or −60 V. When the ADG5401F is powered using a single supply of 25 V or greater, the maximum negative signal level reduces to remain within the 80 V maximum rating. For example, at V_{DD} = +40 V, the maximum negative signal drops from −60 V to −40 V. Construction of the process allows the channel to withstand 80 V across either switch when the switches are open. Note that these overvoltage limits apply whether the power supplies are present or not.

During overvoltage conditions, the leakage current into and out of the S and SFB pins is limited to tens of microamperes and only nanoamperes for the D and DFB pins. This limit protects the switches and connected circuitry from overstresses and restricts the current drawn from the signal source.

ESD Performance

The ADG5401F has an ESD rating of 2 kV for the HBM.

The D and DFB pins have ESD protection diodes to the rails and the voltage at these pins must not exceed the supply voltage. The S and SFB pins have specialized ESD protection that allow the signal voltage to reach ±60 V regardless of the supply voltage level. See Figure 44 for the switch channel overview.

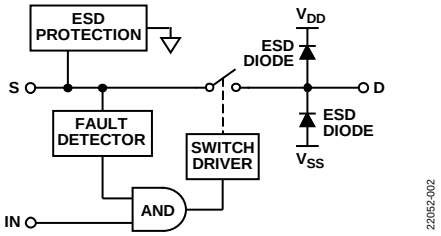

Figure 44. Switch Channel and Control Function

Trench Isolation

In the ADG5401F, an insulating oxide layer (trench) is placed between the N channel DMOS and the P channel DMOS (PDMOS) transistors in the circuit. Parasitic junctions that occur between the transistors in the junction isolated switches are eliminated, and the result is a switch that is latch-up immune under all circumstances. These devices pass the JESD78D latch-up test.

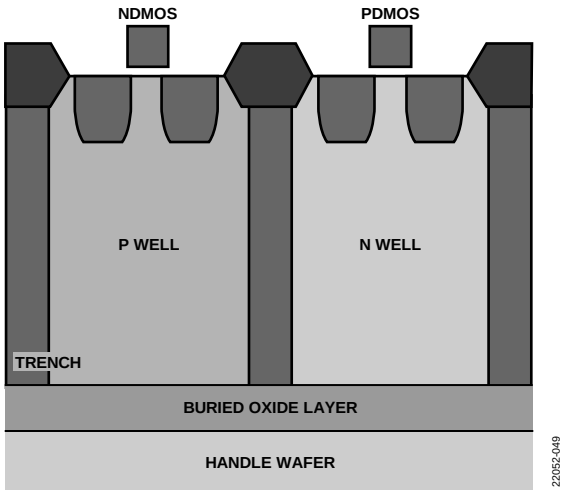

Figure 45. Trench Isolation

OVERVOLTAGE FAULT PROTECTION

When the voltage at the S or SFB input exceeds V_{DD} or V_{SS} by V_T, the switches turn off or, if the device is unpowered, the switches remain off. Both switch inputs remain high impedance regardless of the digital input state or the load resistance, and the output acts as a virtual open circuit. Signal levels up to +60 V and −60 V are blocked in both the powered and unpowered condition as long as the +80 V absolute maximum rating limitation between the S or SFB pin and V_{DD} or V_{SS} pin is met. For example with a +40 V single supply, the overvoltage protection is +60 V and −40 V (see Figure 46).

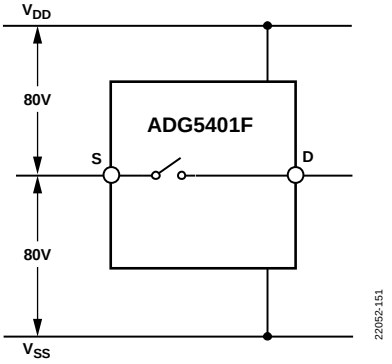

Figure 46. S or SFB to V_{DD} or V_{SS} Maximum Rating

Power-On Protection

To activate the switches, the three following conditions must be meet:

- The minimum supply operating conditions in Table 1.
- The input signal must be between $V_{SS} - V_T$ and $V_{DD} + V_T$.
- The digital logic control input, IN, is on.

When the switches are on, signal levels from V_{SS} up to $V_{DD} - 2$ V are passed.

The switches respond to a voltage on either the S pin or the SFB pin that exceeds V_{DD} or V_{SS} by V_T by turning off. The absolute input voltage limits are −60 V and +60 V, while maintaining an 80 V limit between the S or SFB pin and the supply rails. The switches remain off until the voltage at the S and SFB pins return to between V_{DD} and V_{SS}.

When powered by the ±15 V dual supply, the positive overvoltage response time ($t_{RESPONSE}$) is typically 230 ns, and $t_{RECOVERY}$ is 11.7 µs. These values vary with different supply voltage and output load conditions.

Exceeding ±60 V on either the S or SFB input may damage the ESD protection circuitry on the ADG5401F.

Power Off Protection

When no power supplies are present, the switches remain in an off state and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switches or downstream circuitry. The switch outputs are a virtual open circuit.

The switches remain off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ±60 V are blocked when powered off.

Overvoltage Interrupt Flag

The voltages on the S and SFB inputs of the ADG5401F are continuously monitored, and the active low digital output pin, FF, indicates the fault state.

The voltage on the FF pin indicates if either the S or SFB input pin is experiencing a fault condition. The FF pin is an open-drain output that requires an external pull-up resistor. The output of the FF pin is high when both the S and SFB pins are within the normal operating range. If either the S or SFB pin voltage exceeds the supply voltage (V_{DD} or V_{SS}) by V_T, the FF output provides a low impedance path to GND.

APPLICATIONS INFORMATION

The ADG5401F overvoltage protected switches provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments where overvoltage signals can be present, and the system must remain operational both during and after an overvoltage occurs.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 µF decoupling capacitors are required on both V_{DD} and V_{SS} to GND.

The ADG5401F can operate with bipolar supplies between ±5 V and ±22 V. Note that the V_{DD} and V_{SS} supplies do not have to be symmetrical, but the supply range must not exceed 44 V. The ADG5401F can also operate with single supplies between 8 V and 44 V with V_{SS} connected to GND.

The ADG5401F is fully specified at the ±15 V, ±20 V, +12 V, and +36 V supply ranges.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 47. The ADP5070 (dual switching regulator) generates a positive and negative supply rail for the ADG5401F amplifier and/or a precision converter in a typical signal chain. Also shown in Figure 47 are two optional LDOs, ADP7118 and ADP7182, positive and negative low dropout regulators (LDOs), respectively, that can be used to reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

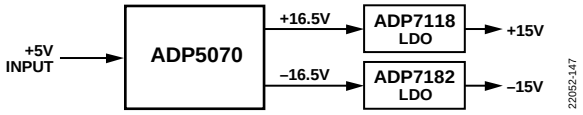

Figure 47. Bipolar Power Solution

Table 11. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7182	−28 V, −200 mA, low noise, LDO linear regulator

POWER SUPPLY SEQUENCING PROTECTION

When the device is off, the switch channels remain open and the signals from −60 V to +60 V can be applied without damaging the device. The switch channels only close when the supplies are connected, a suitable digital control signal is placed on the IN pin, and the signal is within the normal operating range. Note that placing the ADG5401F between external connectors and sensitive components offers protection in systems where a signal is presented to the S or SFB pin before the supply voltages are available.

SIGNAL RANGE

The ADG5401F switches have overvoltage detection circuitry on the S and SFB pins that compares the voltage levels with V_{DD} and V_{SS}. To protect downstream circuitry from overvoltages, supply the ADG5401F with voltages that match the intended signal range. The NDMOS only architecture used in the switches allows signals up to V_{DD} − 2 V to be passed with little distortion. A signal that exceeds the supply rail by V_T is then blocked. This signal block offers protection to both the device and any downstream circuitry.

LOW IMPEDANCE OUTPUT CHANNEL PROTECTION

The ADG5401F can be used as a protective element in signal chain outputs that are sensitive to both channel impedance and overvoltage signals. Traditionally, series resistors are used to limit the current during an overvoltage condition to protect susceptible components.

These series resistors affect the performance of the signal chain and reduce the precision that can be reached. A compromise must be reached on the value of the series resistance that is high enough to sufficiently protect sensitive components but low enough that the precision performance of the signal chain is not sacrificed.

The ADG5401F enables the designer to remove these resistors and retain the precision performance without compromising the protection of the circuit.

INTELLIGENT FAULT DETECTION

The ADG5401F digital output pin (FF) can interface with a microprocessor or control system and be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which the device connects.

The control system can use the digital interrupt to start a variety of actions, such as the following:

- Initiating investigation into the source of the overvoltage fault
- Shutting down critical systems in response to the overvoltage
- Data recorders marking data during these events as unreliable or out of specification

For systems that are sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the ADG5401F powers on and that all input voltages are within the normal operating range before initiating operation.

The FF pin is an open drain that requires an external pull-up resistor, which allows signals to be combined into a single interrupt for larger modules that contain multiple devices.

LARGE VOLTAGE, HIGH FREQUENCY SIGNALS

Figure 28 illustrates the voltage range and frequencies that the ADG5401F can reliably convey. For signals that extend across the full signal range from V_{SS} to V_{DD} − 2 V, keep the frequency below 2.5 MHz. If the required frequency is greater than 2.5 MHz, decrease the signal range appropriately to ensure signal integrity.

AMPLIFIER OR DAC OUTPUT PROTECTION

The ADG5401F has a secondary feedback channel for protecting the amplifier outputs or DAC outputs. The feedback channel is connected between the drain feedback pin (DFB) and the source feedback pin (SFB). This feedback channel has a typical resistance of 0.6 kΩ and can close the feedback loop of an amplifier output or a DAC output (see Figure 48). This feedback loop removes any output error caused by the main channel on resistance.

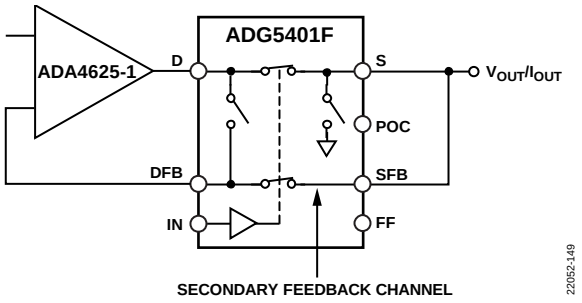

Figure 48. Amplifier Output Protection

The secondary feedback channel is also protected from overvoltages to ±60 V and is controlled by the same switch driver as the main switch channel. If a fault is detected on either the source (S) or source feedback (SFB) pin, both the main switch channel and the feedback channel open, protecting both the amplifier output node and the negative input of the amplifier. For optimal performance, it is recommended to keep the maximum voltage differential between the S and SFB pins to less than 1 V.

If the secondary feedback channel is not required, it is recommended to short the S pin to the SFB pin and the D pin to the DFB pin.

OPEN-LOOP PREVENTION

The open-loop prevention feature is an internal switch in the ADG5401F. When the main switch is disabled, this switch connects the drain (D) of the main switch and the drain of the feedback switch (DFB) (see Figure 49). This internal open-loop prevention switch opens and closes automatically when the main channel switch toggles. This feature stabilizes an amplifier output by preventing the amplifier from going into an open-loop configuration. When the main switch disables in normal operation or in a fault condition, the open-loop prevention switch activates. Note that the open-loop prevention switch is identical to the feedback channel switch.

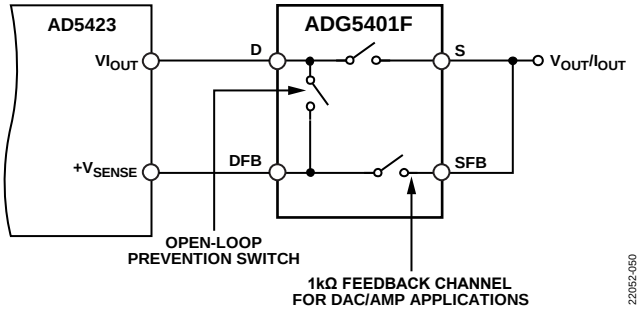

Figure 49. Open-Loop Prevention Feature

POWER-ON CONDITION

The power-on condition feature is a user configurable switch that pulls the source (S) of the switch to ground through a 30 kΩ resistor when the switch is disabled and no fault is present. This feature is enabled with a Logic 0 on the POC pin and disabled with either 5 V on the POC pin or by floating the POC pin.

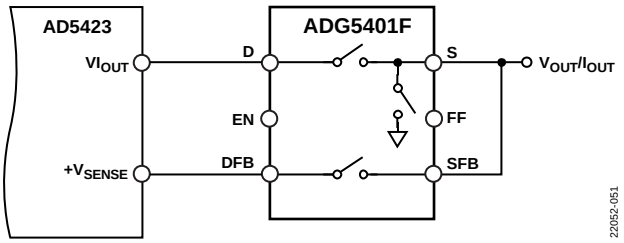

Figure 50. DAC Output Protection

Table 12 details the switch source state when the POC pin is enabled.

Table 12. Switch Source (S) State with POC Enabled

Condition	Switch Source (S)
Switch Disabled, EN = 0	S connected to GND through POC switch (30 kΩ)
Switch Enabled, EN = 1	Connected to D, switch closed
Fault On the Output	Switch open, fault flag asserted
Switch Powering Up	S connected to GND through POC switch (30 kΩ)

SWITCHES IN A KNOWN STATE

If no digital inputs are present on the switch control line (IN), the switches remain in an off state, which prevents unwanted signals passing through the switches.

HIGH VOLTAGE SURGE SUPPRESSION

To achieve protection from high voltage transients, such as IEC 61000-4-2 ESD, IEC 61000-4-4 electrical fast transient (EFT), and IEC 61000-4-5 surge, implement the circuit shown in Figure 51 by using discrete resistors and a transient voltage suppression (TVS) device. Place the resistors inside the feedback loop of the system so that the resistors do not add any error to the system output.

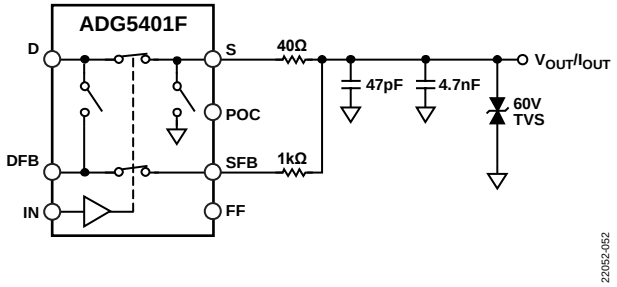

Figure 51. High Voltage Transient Protection

Table 13 details the results achieved by using the discrete protection circuit shown in Figure 51. To replicate the harshest environments , the surge test was performed by zapping the S pin directly through a 40 Ω resistor and a 0.5 µF capacitor coupling network. The EFT test was performed by zapping the S pin directly without any capacitive coupling through cables.

Table 13. High Voltage Transient Protection

IEC 61000-4 Transient	Protection Level (kV)
ESD (Contact)	±6
EFT	±4
Surge	±4

OUTLINE DIMENSIONS

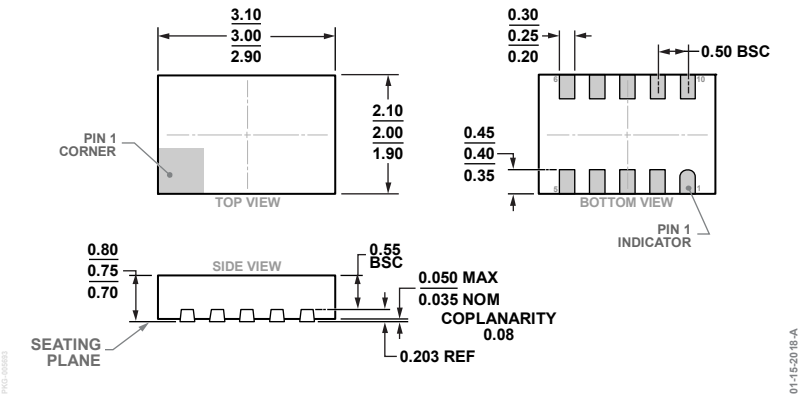

Figure 52. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 2 mm Body and 0.75 mm Package Height
(CP-10-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5401FBCPZ-RL7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-16
EVAL-ADG5401FEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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