Accelerator Series FPGAs: ACT 3 PCI-Compliant Family

Features

- Up to 10,000 Gate Array Equivalent Gates.
- Up to 250 MHz On-Chip Performance.
- 9.0 ns Clock-to-Output.
- Up to 1,153 Dedicated Flip-Flops.
- Up to 228 User-Programmable I/O Pins.
- PCI-Compliant I/O Drivers.
- Four High-Speed, Low-Skew Clocks.
- Highly Predictable, Synthesis-Friendly Architecture Supports High-Level Design Methodologies.
- 100% Module Utilization with Automatic Place and Route Tools.
- Deterministic, User-Controllable Timing via DirectTime Software Tool.
- VHDL and Verilog-HDL Models for PCI Target, Master, and Bridge Functions.

ACT 3 PCI-Compliant Devices

Device	A1460BP	A14100BP
Capacity		
Gate Array Equivalent Gates	6,000	10,000
PLD Equivalent Gates	15,000	25,000
TTL Equivalent Packages (40 Gates)	150	250
20-Pin PAL Equivalent Packages (100 Gates)	60	100
Logic Modules	848	1,377
S-Module	432	697
C-Module	416	680
Dedicated Flip-Flops[1]	768	1,153
User I/Os (Maximum)	168	228
Packages[2] (By Pin Count)		
PQFP	160, 208	—
RQFP	—	208
TQFP	176	—
BGA	225	313
Performance[3] (Maximum, Worst-Case Commercial)		
Chip-to-Chip[4]	97 MHz	93 MHz
Accumulators (16-Bit)	63 MHz	63 MHz
Loadable Counter (16-Bit)	110 MHz	105 MHz
Prescaled Loadable Counters (16-Bit)	150 MHz	150 MHz
Datapath, Shift Registers	150 MHz	150 MHz
Clock-to-Output (Pad-to-Pad)	9.0 ns	9.5 ns

Notes:

1. *One flip-flop per S-module, two flip-flops per I/O module.*
2. *See Product Plan on page 3 for package availability.*
3. *Based on A1460BP-2, and A14100BP-2.*
4. *Clock-to-Output + Set-Up*

Description

Actel enhanced the popular ACT 3 Accelerator Series family of FPGAs to include PCI-compliant I/O drivers. ACT 3 FPGAs are based upon Actel's proprietary antifuse technology and 0.6 micron CMOS process. ACT 3 devices offer a high-performance, PCI-compliant programmable solution. The ACT 3 PCI-compliant family delivers 200 MHz on-chip operation and 9.0 nanosecond clock-to-output performance with capacities spanning from 6,000 to 10,000 gate array equivalent gates. The PCI-compliant ACT 3 devices are denoted with a "BP" designator and are shown in the ordering information chart.

Actel's ACT 3 PCI-compliant devices provide a high-capacity, synthesis-friendly programmable solution to PCI applications. The following headings detail the pertinent PCI Local Bus Specifications along with the corresponding ACT 3 parameters. The section numbers in the notes denote the pertinent section in the PCI Local Bus Specification version 2.1. ACT 3 devices comply 100% to the electrical and timing specifications detailed in the PCI specification. However, as with all programmable logic devices, the performance of the final product depends upon the user's design and optimization techniques.

Predictable Performance* (Worst-Case Commercial)

Accumulators (16-Bit)	63 MHz
Loadable Counters (16-Bit)	110 MHz
Prescaled Loadable Counters (16-Bit)	250 MHz
Shift Registers	250 MHz

Ordering Information

A14100 BP – RQ 208 C

Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)

Package Lead Count

Package Type
PQ = Plastic Quad Flatpack
RQ = Plastic Power Quad Flatpack
TQ = Thin (1.4 mm) Quad Flatpack
BG = Plastic Ball Grid Array

Speed Grade
Std = Standard Speed
–1 = Approximately 15% Faster than Standard
–2 = Approximately 25% Faster than Standard
–3 = Approximately 35% Faster than Standard

Die Revision

Part Number
A1460BP = 6000 Gates
A14100BP = 10000 Gates

Product Plan

	Speed Grade*				Application	
	Std	–1	–2	–3	C	I
A1460BP Device						
160-Pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	P
176-Pin Thin Quad Flatpack (TQFP)	P	P	P	P	P	P
208-Pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	P
225-Pin Plastic Ball Grid Array (BGA)	P	P	P	P	P	—
A14100BP Device						
208-Pin Power Quad Flatpack (RQFP)	✔	✔	✔	✔	✔	P
313-Pin Plastic Ball Grid Array (BGA)	P	P	P	P	P	—

Note: *P = Planned, ✔ = Availiable.*

Plastic Device Resources

			User I/Os				
			PQFP, RQFP		TQFP	BGA	
Device Series	**Logic Modules**	**Gates**	**160-Pin**	**208-Pin**	**176-Pin**	**225-Pin**	**313-Pin**
A1460BP	848	6000	131	167	151	168	—
A14100BP	1377	10000	—	175	—	—	228

Pin Description

CLKA Clock A (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

HCLK Dedicated (Hard-Wired) Array Clock (Input)

TTL clock input for sequential modules. This input is directly wired to each S-module, and offers clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

IOCLK Dedicated (Hard-Wired) I/O Clock (Input)

TTL clock input for I/O modules. This input is directly wired to each I/O module, and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer Series software.

IOPCL Dedicated (Hard-Wired) I/O Preset/Clear (Input)

TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

NC No Connection

This pin is not connected to circuitry within the device.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide ActionProbe capability, the MODE pin should be terminated to GND through a 10K resistor, allowing the MODE pin to be pulled HIGH when required.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

DCLK Diagnostic Clock (Input)

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRA **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The PRA pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The PRB pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} **5V Supply Voltage**

HIGH supply voltage.

GND **Ground**

LOW supply voltage.

Architecture

This section of the data sheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, routing structure, antifuses, and special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: logic modules, I/O modules, I/O pad drivers, routing tracks, clock networks, and programming and test circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 1.

Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules. The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input ANDs and 5-input ORs, and is available for use as a CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module. S-modules consist of a full C-module driving a flip-flop, allowing an additional level of logic to be implemented without additional propagation delay. It is available for use as DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module pairs; module pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types: CC, CS, SC, and SS. The C-module implements the following function:

Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11

where: S0 = A0 * B0 and S1 = A1 + B1

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can implement any function implemented by the C-module, allowing complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series development system will automatically combine any C-module macro driving an S-module macro into the S-module, freeing up a logic module and eliminating a module delay.

The clear input (CLR) is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLK0, CLK1, or HCLK. The C-module and S-module functional descriptions are shown in Figures 2 and 3. The clock selection multiplexor selects the clock input to the S-module.

I/O Modules

I/O modules provide an interface between the array and the I/O pad drivers. I/O modules are located in the array and access the routing channels in a fashion similar to logic modules. There are two types of I/O modules: side/side and top/bottom. The I/O module schematic is shown in Figure 4. UO1 and UO2 are inputs from the routing channel: one for the routing channel above and one for the routing channel below the module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input. The signals DataIn and DataOut connect to the I/O pad driver. Each I/O module contains two D-type flip-flops, and each flip-flop is connected to the dedicated I/O clock (IOCLK).

Each flip-flop can be bypassed by non-sequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated

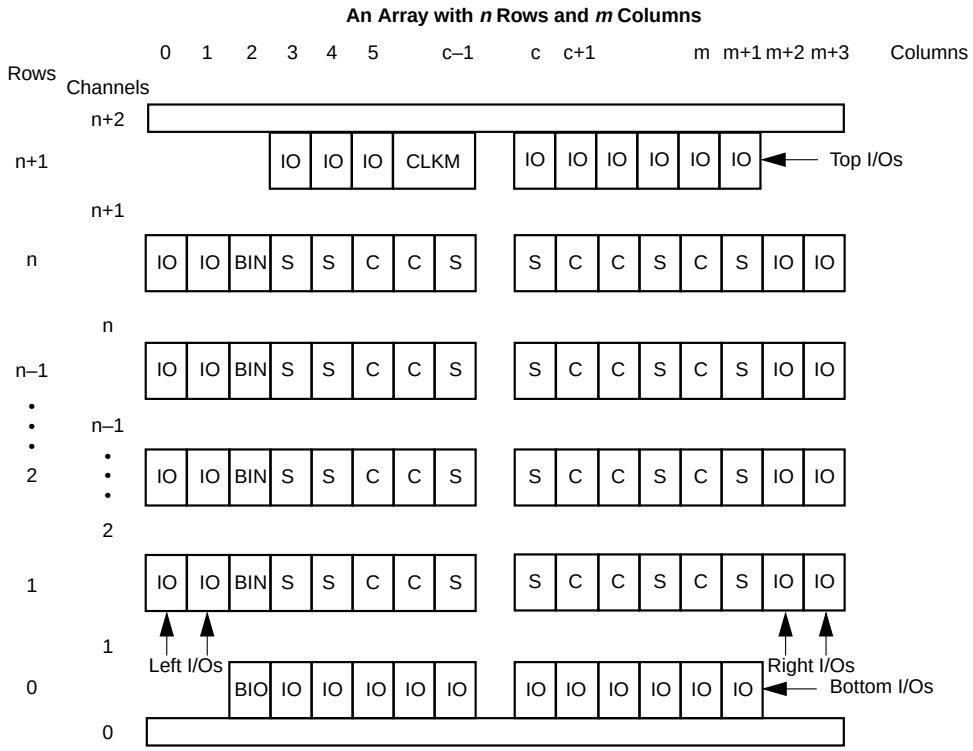


Figure 1 • *Generalized Floor Plan of ACT 3 Device*

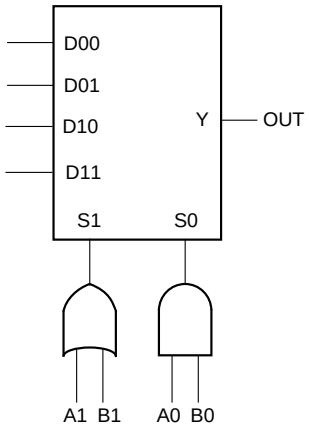


Figure 2 • *C-Module Diagram*

preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O-module-by-I/O-module basis.

The I/O module output Y is used to bring pad signals into the array *or* to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tri-state. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 5.

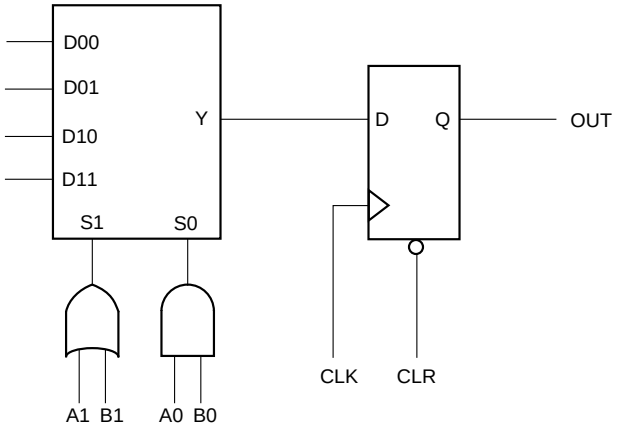


Figure 3 • *S-Module Diagram*

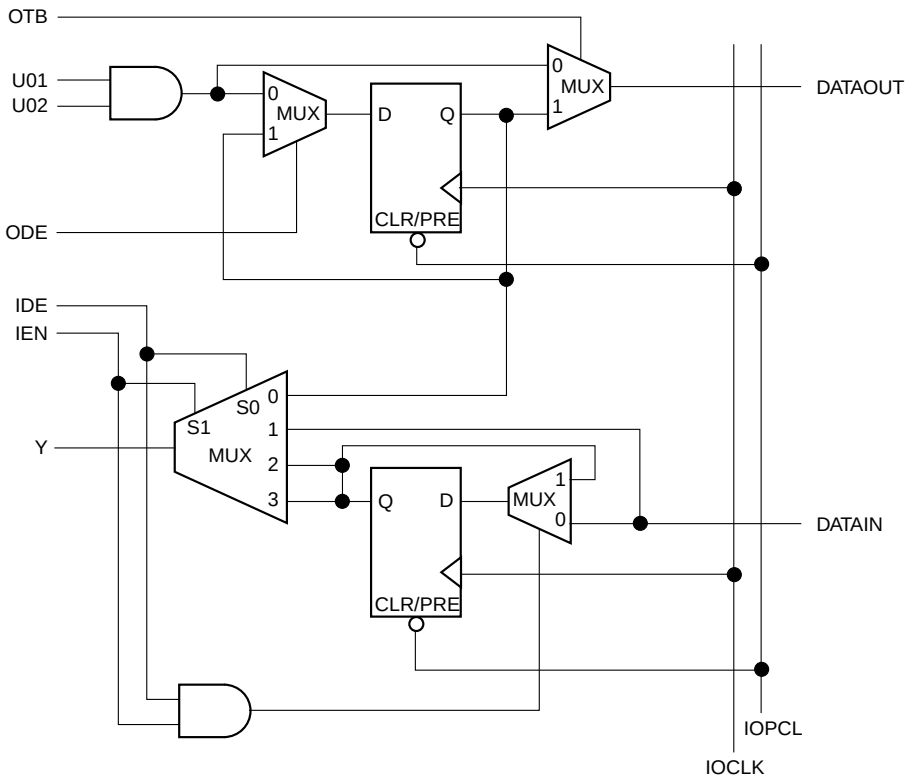


Figure 4 • *Function Diagram for I/O Module*

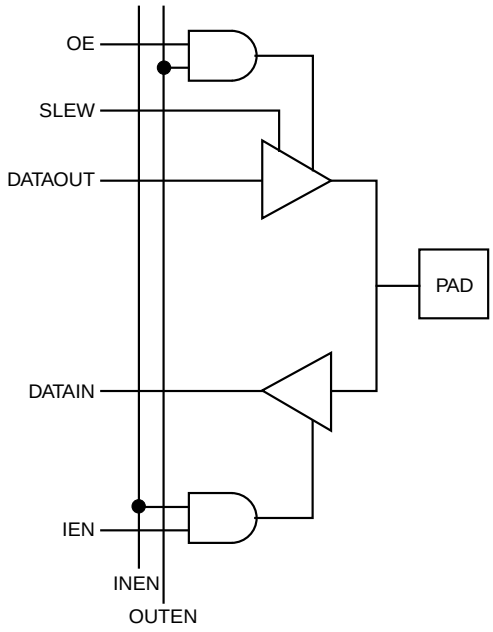


Figure 5 • *Function Diagram for I/O Pad Driver*

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing, and function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user-programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general-purpose routed networks. The high-performance networks function up to 200 MHz, while the general-purpose routed networks function up to 150 MHz.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and predictable performance. Dedicated clock networks contain no programming elements in the path from the I/O pad driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

Routed Clocks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal, and may be driven as follows (see Figure 6):

- Externally from the CLKA Pad
- Externally from the CLKB Pad
- Internally from the CLKINA Input
- Internally from the CLKINB Input

The clock modules are located in the top row of the I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user may use either CLK0 or CLK1. Routed clocks can also be used to drive high-fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

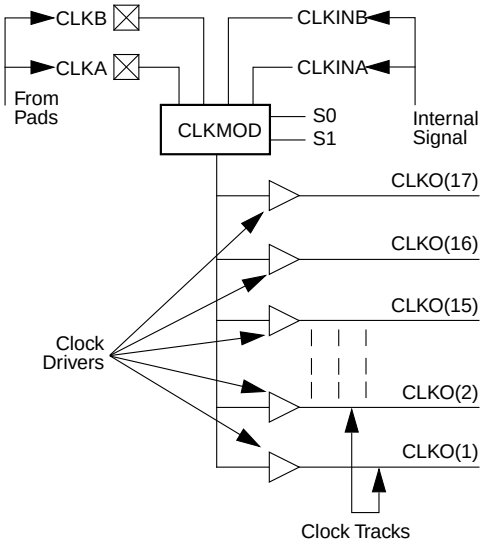


Figure 6 • *Clock Networks*

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules, and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third of the row's length is considered a long horizontal segment. A typical channel is shown in Figure 7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks, and for power and ground tie-off tracks.

Vertical Routing

Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments, with each segment in an input track dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

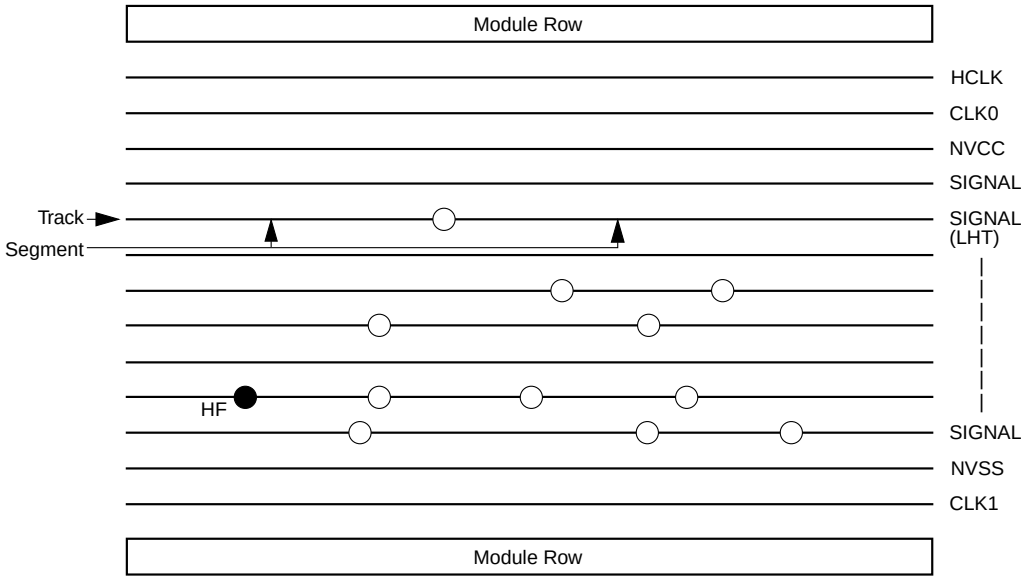


Figure 7 • *Horizontal Routing Tracks and Segments*

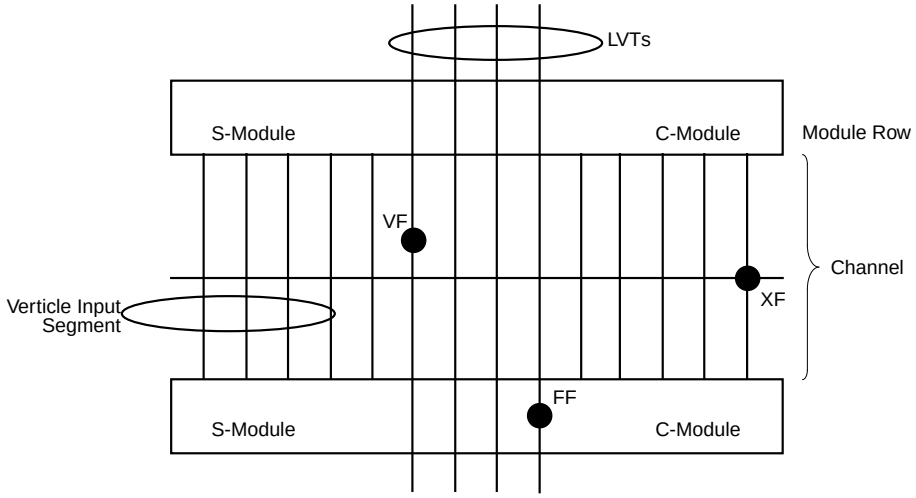


Figure 8 • *Vertical Routing Tracks and Segments*

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the "normally closed" fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures, as well as an efficient programming architecture. The structure is highly testable because there are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed, as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. The physical structure of the antifuse is identical in each case; only the usage differs. Table 1 shows four types of antifuses.

Table 1 • *Antifuse Types*

XF	Horizontal-to-Vertical Connection
HF	Horizontal-to-Horizontal Connection
VF	Vertical-to-Vertical Connection
FF	"Fast" Vertical Connection

Examples of all four types of connections are shown in Figures 7 and 8.

Module Interface

Connections to logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 9.

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to non-dedicated segments called long vertical tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in

the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general, every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, a subset of the input has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar in all ACT family devices. The ACT 3 family also includes support for two ActionProbe circuits, allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins PRA and PRB.

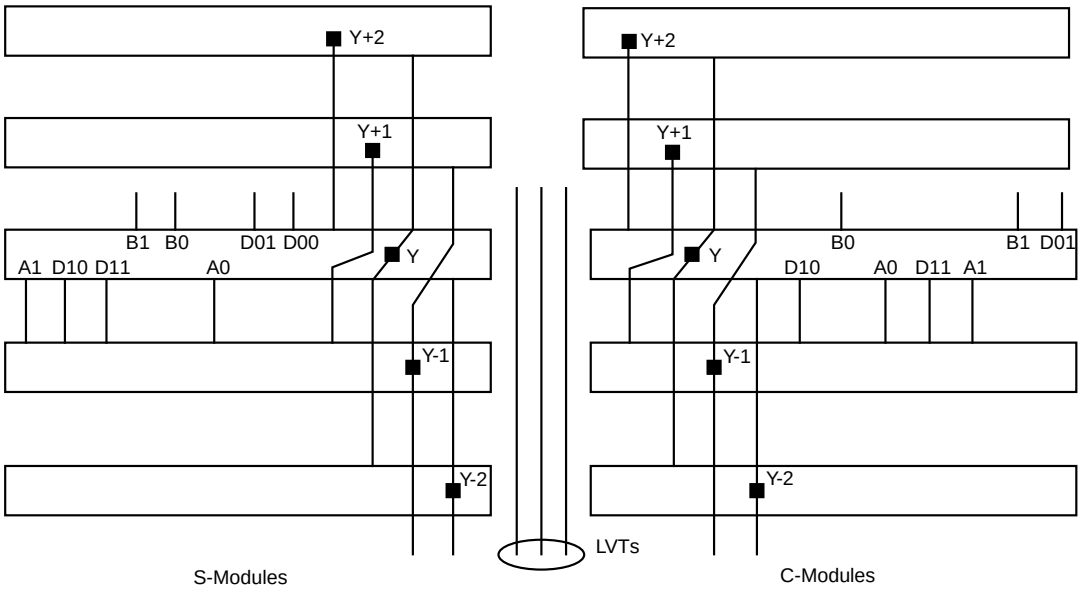


Figure 9 • *Logic Module Routing Interface*

5V Operating Conditions

Absolute Maximum Ratings[1]

Free Air Temperature Range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diodes will forward-bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
5V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

The PCI bus specifies I/O drivers in terms of the DC and AC characteristics. However, since the PCI bus drivers spend a relatively large proportion of time transitioning from one power rail to the other, PCI drivers are primarily characterized by their V/I curves (Tables 2 and 3).

Output Drive Characteristics for 5.0V Signaling

ACT 3 PCI device I/O drivers were designed specifically for high-performance PCI systems. Figures 10 and 11 show the typical output drive characteristics of the 5.0V ACT 3 devices. ACT 3 output drivers are compliant with the PCI Local Bus Specification.

Table 2 • *DC Specification for 5.0V Signaling*[1]

			PCI		ACT 3		
Symbol	**Parameter**	**Condition**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**
V_{CC}	Supply Voltage		4.75	5.25	4.75	5.25[2]	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	0.8	–0.3	0.8	V
I_{IH}	Input High Current	V_{IN} = 2.7		70	—	10	µA
I_{IL}	Input Low Current	V_{IN}=0.5		–70	—	–10	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		3.7		V
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55	—	0.33	V
C_{IN}	Input Pin Capacitance			10	—	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L_{PIN}	Pin Inductance			20	—	< 8 nH[3]	nH

Notes:

1. *PCI Local Bus Specification Section 4.2.1.1.*
2. *Maximum rating for V_{CC} –0.5V to 7.0V. Refer to Accelerator Series FPGAs ACT 3 family data sheet.*
3. *Dependent upon the chosen package. PCI recommends QFP packaging to reduce pin inductance and capacitance.*

Table 3 • *AC Specifications for 5.0V Signaling*[1]

			PCI		ACT 3		
Symbol	**Parameter**	**Condition**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**
I_{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	$-25 + (V_{IN} + 1) / 0.015$		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4V to 2.4V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Lall Slew Rate	2.4V to 0.4V load	1	5	2.8	4.3	V/ns

Note:

1. *PCI Local Bus Specification Section 4.2.1.2.*

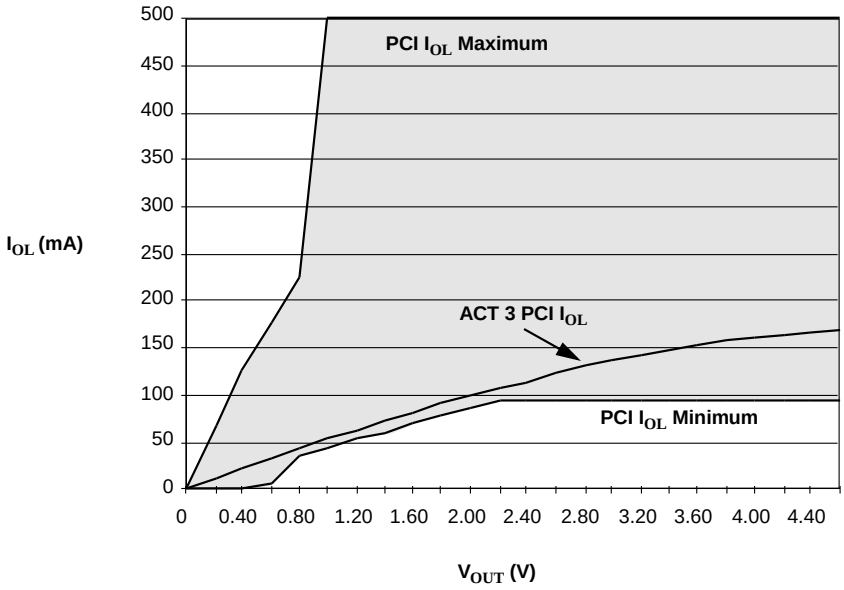


Figure 10 • *Typical Output Drive Characteristics (Based upon simulation data)*

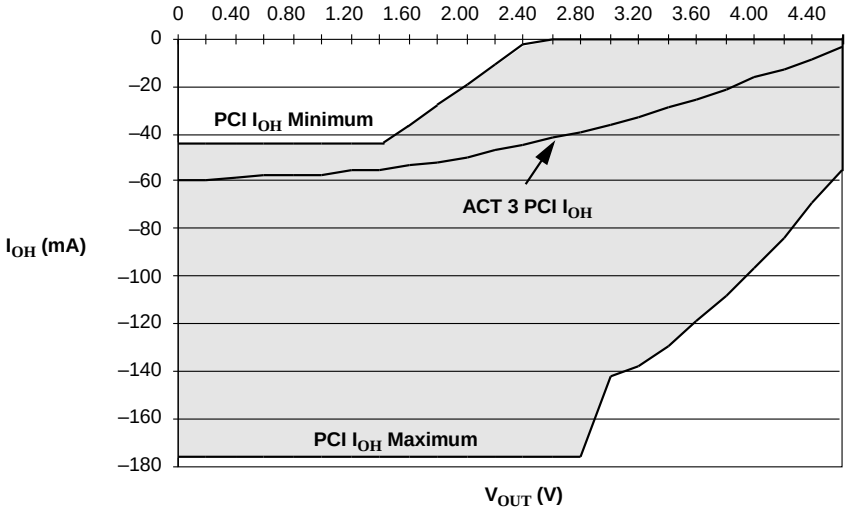


Figure 11 • *Typical Output Drive Characteristics (Based upon simulation data)*

System Timing Specification

Tables 4 and 5 list the critical PCI timing parameters and the corresponding timing parameter for the ACT 3 PCI-compliant devices.

PCI Models

Actel provides synthesizable VHDL and Verilog-HDL models for a PCI target interface, a PCI master interface, and a PCI-to-PCI bridge interface. Consult your local Actel sales representative for more details.

Table 4 • *Clock Specification for 33 MHz PCI*[1]

		PCI		ACT 3		
Symbol	**Parameter**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**
T_{CYC}	CLK Cycle Time	30	—	4.0	—	ns
T_{HIGH}	CLK High Time	11	—	1.9	—	ns
T_{LOW}	CLK Low Time	11	—	1.9	—	ns

Note:

1. *PCI Local Bus Specification Section 4.2.3.1.*

Table 5 • *Timing Parameters for 33 MHz PCI*[1]

		PCI		ACT 3		
Symbol	**Parameter**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Units**
T_{VAL}	CLK to Signal Valid—Bused Signals	2	11	2.0	9.0	ns
$T_{VAL(PTP)}$	CLK to Signal Valid—Point-to-Point	2	12	2.0	9.0	ns
T_{ON}	Float to active	2	—	2.0	4.0	ns
T_{OFF}	Active to Float	—	28	—	8.3[2]	ns
T_{SU}	Input Set-Up Time to CLK—Bused Signals	7	—	1.5	—	ns
$T_{SU(PTP)}$	Input Set-Up Time to CLK—Point-to-Point	10, 12	—	1.5	—	ns
T_{H}	Input Hold to CLK	0	—	0	—	ns

Notes:

1. *For information only. These values represent registered I/O timing used in the PCI macro implementation for an A1460BP-2 device. Please see the PCI macro specification for more information on timing and speed bin requirements.*
2. *T_{OFF} is system dependent. ACT 3 PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. Junction Temp. (°C)} - \text{Max. Ambient Temp. (°C)}}{\theta_{ja}\ (\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{25\text{°C/W}} = 3.2\ \text{W}$$

Package Type[1]	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Plastic Quad Flatpack	160	10	33	26	°C/W
	208	10	33	26	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note:

1. *Maximum power dissipation in still air for 160-pin PQFP package is 2.4 watts, 208-pin PQFP package is 2.4 watts, 100-pin PQFP package is 1.6 watts, 100-pin VQFP package is 1.9 watts, 176-pin TQFP package is 2.5 watts, 84-pin PLCC package is 2.2 watts, 208-pin RQFP package is 4.7 watts, 225-pin BGA package is 3.2 watts, 313-pin BGA package is 3.5 watts.*

Power Dissipation

$$P = [I_{CC\ standby} + I_{active}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M \quad (1)$$

Where:

$I_{CC\ standby}$ is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst-case conditions.

I_{CC}	V_{CC}	Power
2mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving HIGH or LOW and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving LOW, and 140 mW with all outputs driving HIGH. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This frequency-dependent component is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 2.

$$\text{Power}\ (\mu\text{W}) = C_{EQ} * V_{CC}^2 * F \quad (2)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC} active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent, allowing the results to be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

Modules (C_{EQM})	6.7
Input Buffers ($_{CEQI}$)	7.2
Output Buffers (C_{EQO})	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7
I/O Clock Buffer Loads (C_{EQCI})	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 3 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * CEQCD * f_{s1})_{dedicated\_Clk} + (s_2 * CEQCI * f_{s2})_{IO\_Clk}] \quad (3)$$

Where:

m = Number of logic modules switching at f_m
n = Number of input buffers switching at f_n
p = Number of output buffers switching at f_p
q_1 = Number of clock loads on the first routed array clock
q_2 = Number of clock loads on the second routed array clock
r_1 = Fixed capacitance due to first routed array clock
r_2 = Fixed capacitance due to second routed array clock
s_1 = Fixed number of clock loads on the dedicated array clock
s_2 = Fixed number of clock loads on the dedicated I/O clock
C_{EQM} = Equivalent capacitance of logic modules in pF
C_{EQI} = Equivalent capacitance of input buffers in pF
C_{EQO} = Equivalent capacitance of output buffers in pF
C_{EQCR} = Equivalent capacitance of routed array clock in pF
C_{EQCD} = Equivalent capacitance of dedicated array clock in pF
C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF
C_L = Output lead capacitance in pF
f_m = Average logic module switching rate in MHz
f_n = Average input buffer switching rate in MHz
f_p = Average output buffer switching rate in MHz
f_{q1} = Average first routed array clock rate in MHz
f_{q2} = Average second routed array clock rate in MHz
f_{s1} = Average dedicated array clock rate in MHz
f_{s2} = Average dedicated I/O clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1460BP	165	165
A14100BP	195	195

Fixed Clock Loads (s_1/s_2)

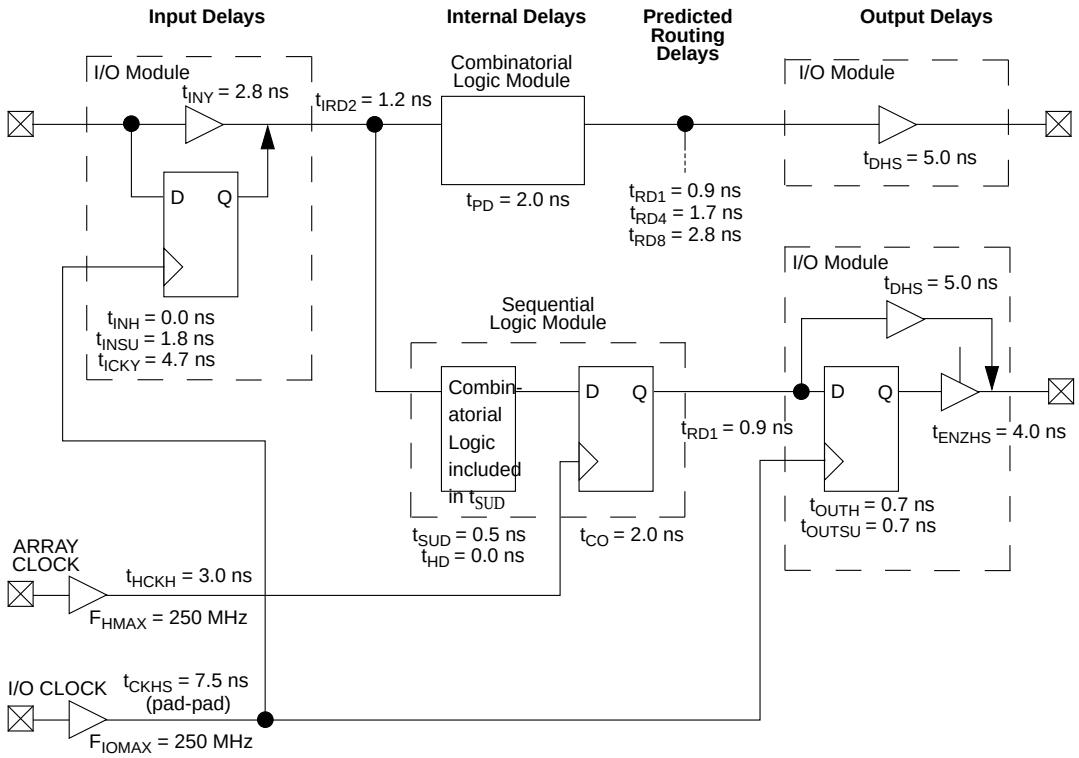
Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
A1460BP	432	168
A14100BP	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios that can be generally used to predict the upper limits of power dissipation.

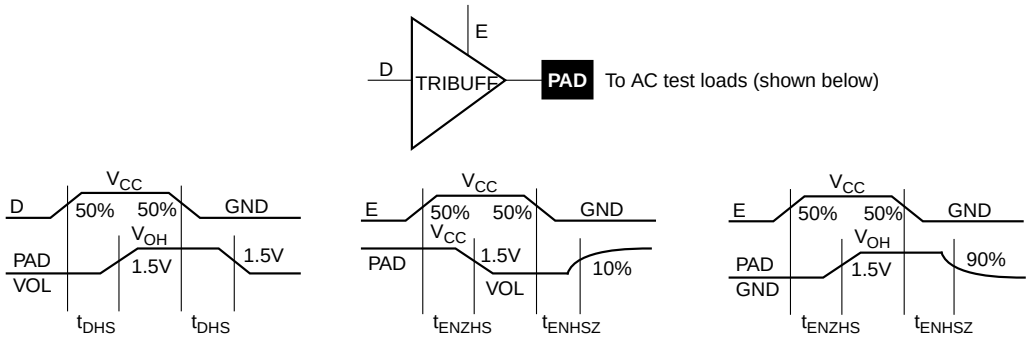
Logic Modules (m)	=	80% of Modules
Inputs Switching (n)	=	# Inputs/4
Outputs Switching (p)	=	# Output/4
First Routed Array Clock Loads (q_1)	=	40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	=	40% of Sequential Modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F/2
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	F
Average Dedicated I/O Clock Rate (f_{s2})	=	F

ACT 3 Timing Model*

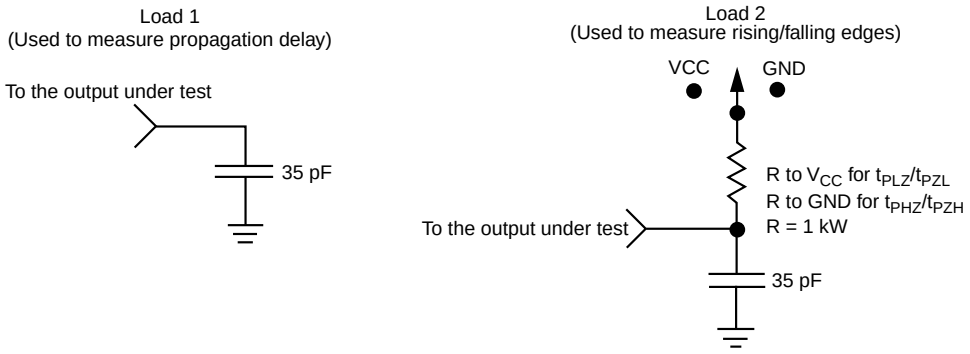


**Values shown for A1425A-3.*

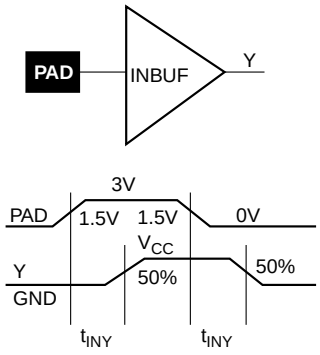
Output Buffer Delays



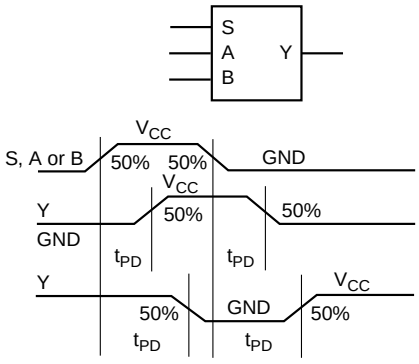
AC Test Loads



Input Buffer Delays

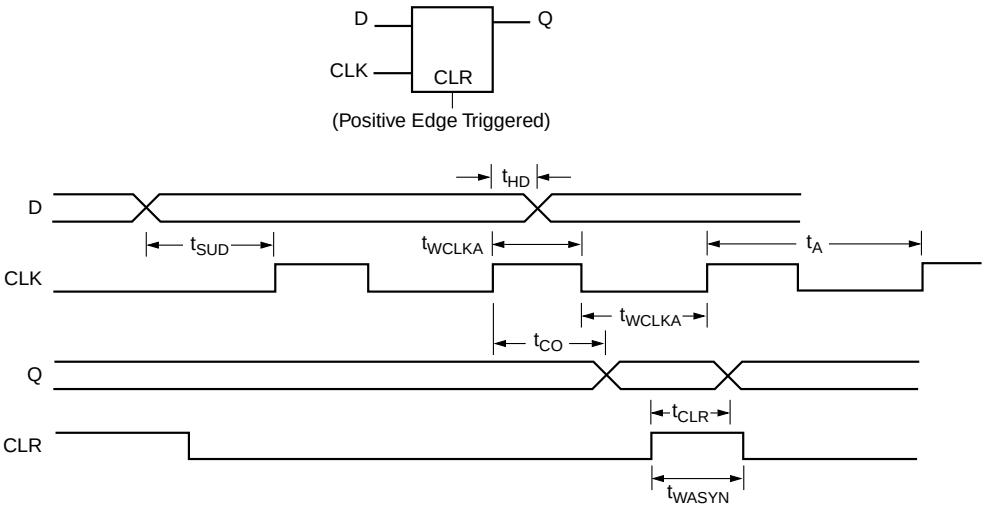


Module Delays

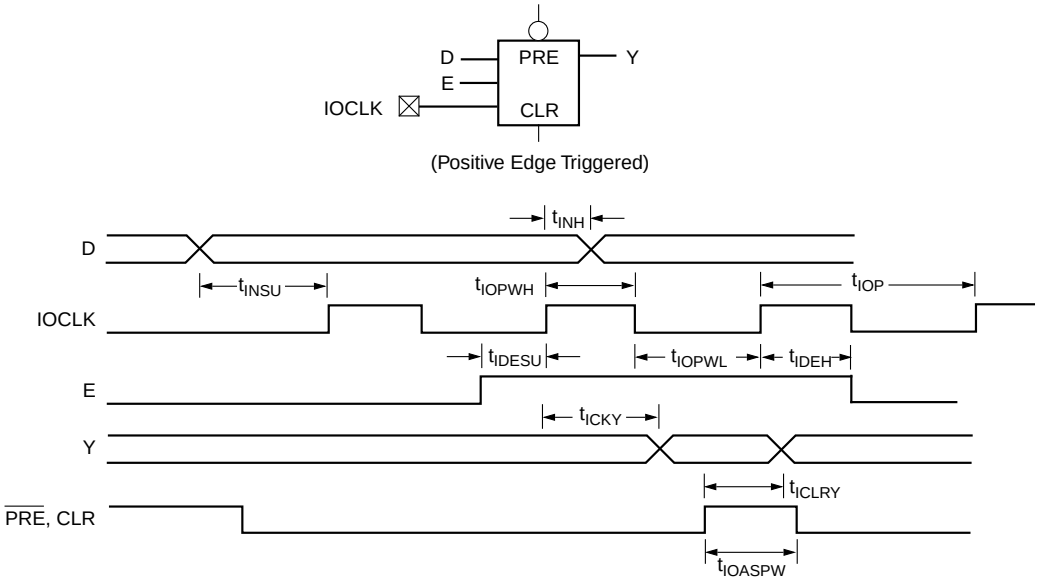


Sequential Module Timing Characteristics

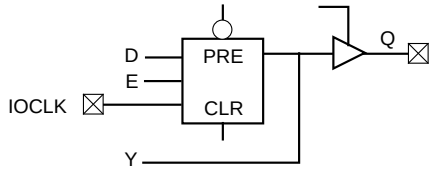
Flip-Flops



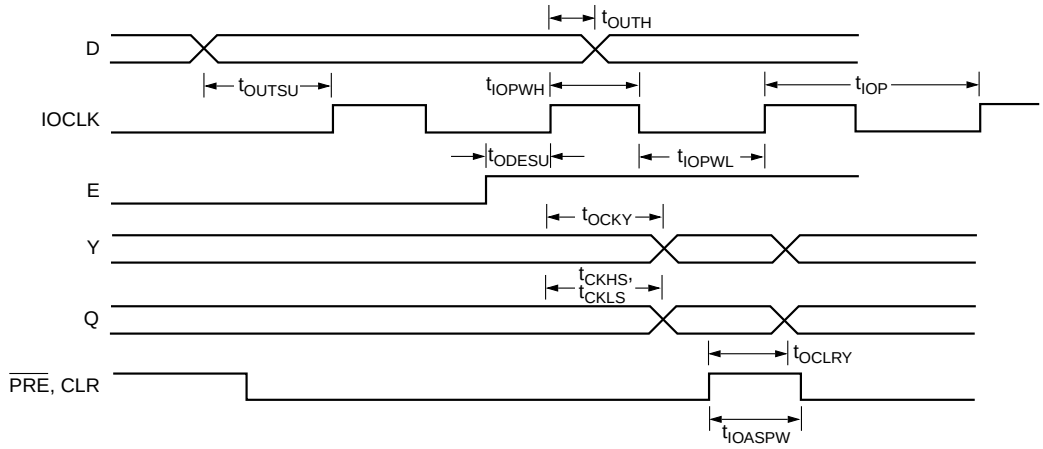
I/O Module: Sequential Input Timing Characteristics



I/O Module: Sequential Output Timing Characteristics



(Positive Edge Triggered)



Predictable Performance: Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track.

The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses offer nominal levels of 200Ω resistance and 6 femtofarad (fF) capacitance per antifuse.

The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

Table 6 • *Logic Module and Routing Delay by Fanout (ns) (Worst-Case Commercial Conditions)*

Speed	FO=1	FO=2	FO=3	FO=4	FO=8
–3	2.9	3.2	3.4	3.7	4.8

Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of the nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 14 ns delay, and is represented statistically in higher fanout (FO=8) routing delays (noted in the Specifications section).

Timing Derating

ACT 3 devices are manufactured in a CMOS process; therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Timing Derating Factor (Temperature and Voltage)

	Industrial		Military	
	Min.	Max.	Min.	Max.
(Commercial Minimum/Maximum Specification) x	0.66	1.07	0.63	1.17

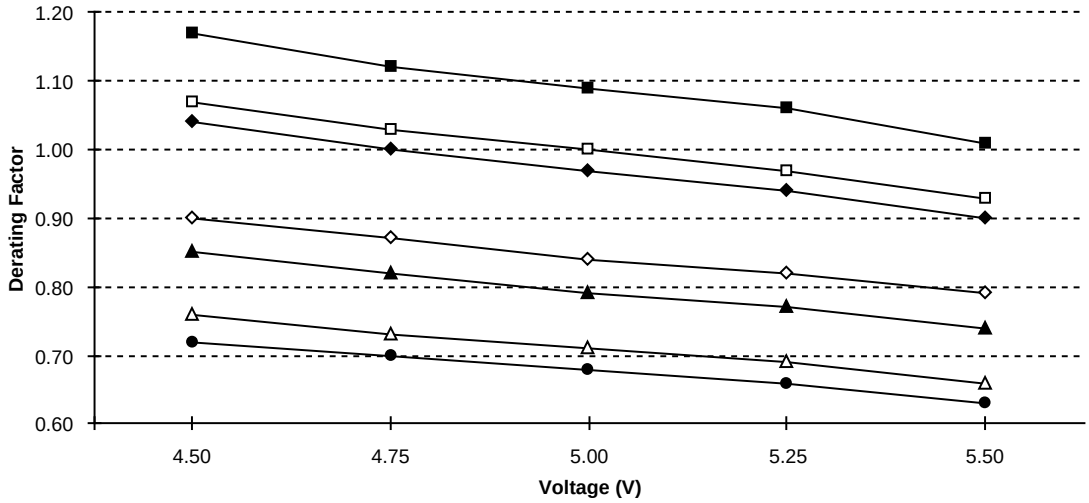
Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0V)

(Commercial Maximum Specification) x	0.85

Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 4.75V, 70°C)

	–55	–40	0	25	70	85	125
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.17
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01

Junction Temperature and Voltage Derating Curves (Normalized to Worst-Case Commercial, T_J = 4.75V, 70°C)



Note: *This derating factor applies to all routing and propagation delays.*

A1460BP Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)[1]

Logic Module Propagation Delays[2]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0	ns
Predicted Routing Delays[3]										
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5	ns
t_{RD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2	ns
Logic Module Sequential Timing										
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		200		150		125		100	MHz

Notes:

1. *V_{CC} = 3.0V for 3.3V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$ or $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460BP Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{IRD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5	ns
t_{IRD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2	ns
I/O Module Sequential Timing										
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Set-Up (w.r.t. IOCLK Pad)	1.3		1.5		1.8		2.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Set-Up (w.r.t. IOCLK Pad)	5.8		6.5		7.5		8.6		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		ns
t_{OUTSU}	Output F-F Data Set-Up (w.r.t. IOCLK Pad)	0.7		0.8		0.9		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.3		0.4		0.4		0.5		ns
t_{ODESU}	Output Data Enable Set-Up (w.r.t. IOCLK Pad)	1.3		1.5		1.7		2.0		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460BP Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.8		8.7		9.9		11.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.0		11.5	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0	ns
d_{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07	ns/pF
I/O Module – CMOS Output Timing[1]										
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.1		13.8	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05	ns/pF

Note:

1. Delays based on 35pF loading.

A1460BP Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) I/O Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	2.4		3.2		3.8		4.8		ns
t_{IOPWL}	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.2		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.6		0.6		0.6		0.6	ns
t_{IOP}	Minimum Period	5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		200		150		125		100	MHz
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input Low to High (Pad to S-Module Input)		3.7		4.1		4.7		5.5	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		3.7		4.1		4.7		5.5	ns
t_{HPWH}	Minimum Pulse Width High	2.4		3.2		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.6		0.6	ns
t_{HP}	Minimum Period	5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		200		150		125		100	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (FO=256)		6.0		6.8		7.7		9.0	ns
t_{RCKL}	Input High to Low (FO=256)		6.0		6.8		7.7		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	4.1		4.5		5.4		6.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	4.1		4.5		5.4		6.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.2		1.4		1.6		1.8	ns
t_{RP}	Minimum Period (FO=256)	8.3		9.3		11.1		12.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		120		105		90		80	MHz
Clock-to-Clock Skews										
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.7	0.0	1.7	0.0	1.7	0.0	1.7	ns
	(FO = 216)	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.3	0.0	1.0	0.0	1.0	0.0	1.0	ns
	(FO = 216)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35pF loading.

A14100BP Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75V, T_J = 70°C)[1]

Logic Module Propagation Delays[2]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0	ns
Predicted Routing Delays[3]										
t_{RD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5	ns
t_{RD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2	ns
Logic Module Sequential Timing										
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.5		0.5		ns
t_{SUD}	Latch Data Input Set-Up	0.5		0.6		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.5		0.5		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		200		150		125		100	MHz

Notes:

1. *V_{CC} = 3.0V for 3.3V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100BP Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		0.9		1.0		1.1		1.3	ns
t_{IRD2}	FO=2 Routing Delay		1.2		1.4		1.6		1.8	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{IRD4}	FO=4 Routing Delay		1.7		1.9		2.2		2.5	ns
t_{IRD8}	FO=8 Routing Delay		2.8		3.2		3.6		4.2	ns
I/O Module Sequential Timing										
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Set-Up (w.r.t. IOCLK Pad)	1.2		1.4		1.5		1.8		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Set-Up (w.r.t. IOCLK Pad)	5.8		6.5		7.5		8.6		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	0.7		0.8		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Set-Up (w.r.t. IOCLK Pad)	0.7		0.8		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.3		0.4		0.5		0.5		ns
t_{ODESU}	Output Data Enable Set-Up (w.r.t. IOCLK Pad)	1.3		1.5		2.0		2.0		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100BP Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0	ns
d_{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07	ns/pF
I/O Module – CMOS Output Timing[1]										
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05	ns/pF

Note:

1. Delays based on 35pF loading.

A14100BP Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

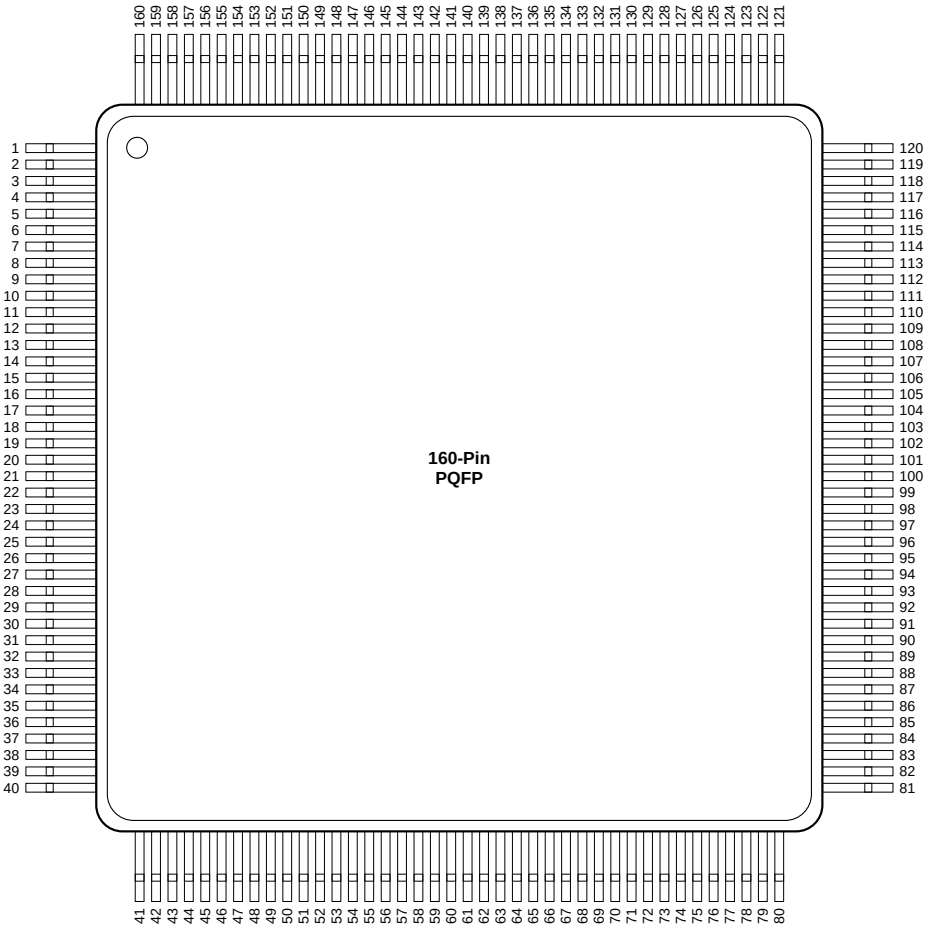
Dedicated (Hard-Wired) I/O Clock Network		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		ns
t_{IOPWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.6		0.6		0.7		0.8	ns
t_{IOP}	Minimum Period	5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		200		150		125		100	MHz
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input Low to High (Pad to S-Module Input)		3.7		4.1		4.7		5.5	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		3.7		4.1		4.7		5.5	ns
t_{HPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.7		0.8	ns
t_{HP}	Minimum Period	5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		200		150		125		100	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (FO=256)		6.0		6.8		7.7		9.0	ns
t_{RCKL}	Input High to Low (FO=256)		6.0		6.8		7.7		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	4.1		4.5		5.4		6.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	4.1		4.5		5.4		6.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.2		1.4		1.6		1.8	ns
t_{RP}	Minimum Period (FO=256)	8.3		9.3		11.1		12.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		120		105		90		80	MHz
Clock-to-Clock Skews										
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.7	0.0	17	0.0	1.7	0.0	1.7	ns
	(FO = 350)	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.3	0.0	1.0	0.0	1.0	0.0	1.0	ns
	(FO = 350)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35pF loading.

Package Pin Assignments

160-Pin PQFP (Top View)



160-Pin PQFP

Pin Number	A1460BP Function
1	GND
2	SDI, I/O
5	I/O
9	MODE
10	V_{CC}
14	I/O
15	GND
18	V_{CC}
19	GND
20	I/O
24	I/O
27	I/O
28	V_{CC}
29	V_{CC}
40	GND
41	I/O
43	I/O
45	I/O
46	V_{CC}
47	I/O
49	I/O
51	I/O
53	I/O
58	PRB, I/O
59	GND
60	V_{CC}
62	HCLK, I/O
63	GND
74	I/O
75	V_{CC}
76	I/O
77	I/O
78	I/O
80	IOPCL, I/O
81	GND

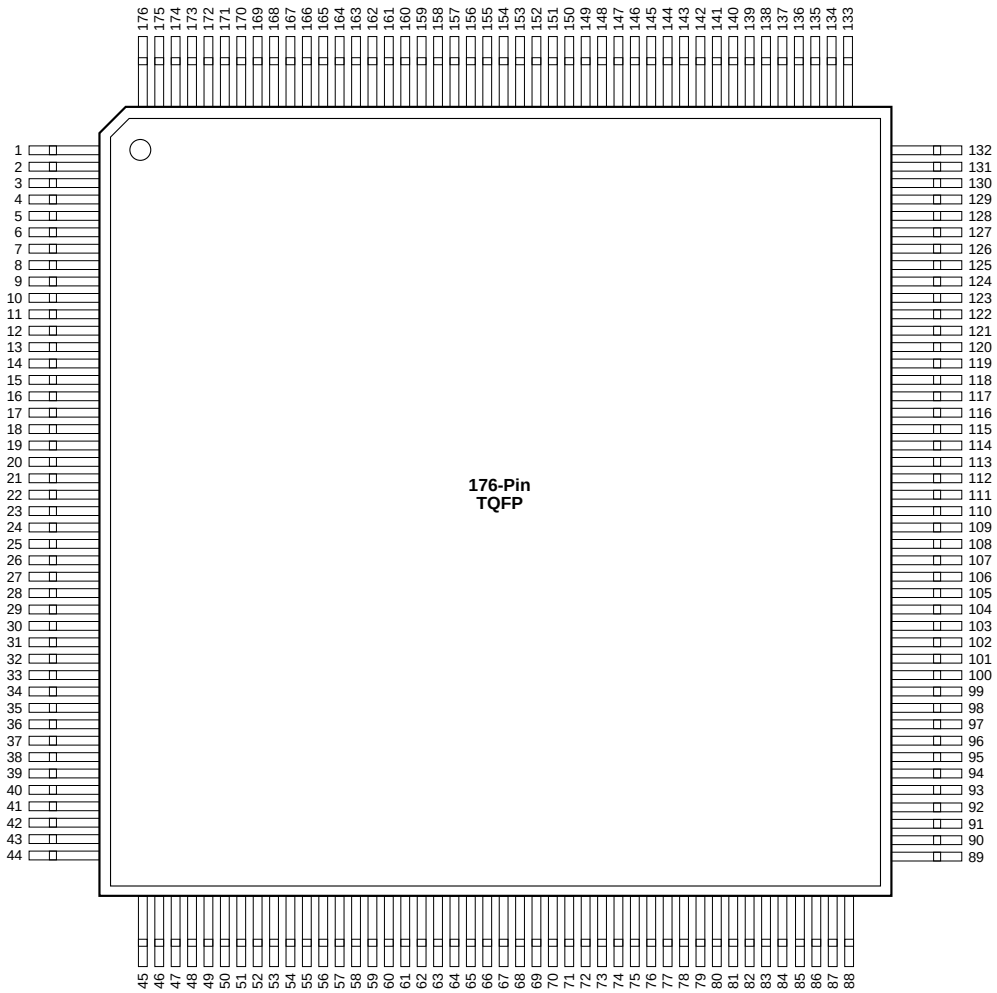
Pin Number	A1460BP Function
90	V_{CC}
91	V_{CC}
92	I/O
93	I/O
98	GND
99	V_{CC}
100	I/O
103	GND
107	I/O
109	I/O
110	V_{CC}
111	GND
112	V_{CC}
113	I/O
119	I/O
120	IOCLK, I/O
121	GND
124	I/O
127	I/O
136	CLKA, I/O
137	CLKB, I/O
138	V_{CC}
139	GND
140	V_{CC}
141	GND
142	PRA, I/O
143	I/O
145	I/O
147	I/O
149	I/O
151	I/O
153	I/O
154	V_{CC}
160	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC: Denotes "No Connection"*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

176-Pin TQFP (Top View)



176-Pin TQFP

Pin Number	A1460BP Function
1	GND
2	SDI, I/O
10	MODE
11	V_{CC}
20	I/O
21	GND
22	V_{CC}
23	GND
32	V_{CC}
33	V_{CC}
44	GND
49	I/O
51	I/O
63	I/O
64	PRB, I/O
65	GND
66	V_{CC}
67	V_{CC}
69	HCLK, I/O
82	I/O
83	I/O
88	IOPCL, I/O
89	GND

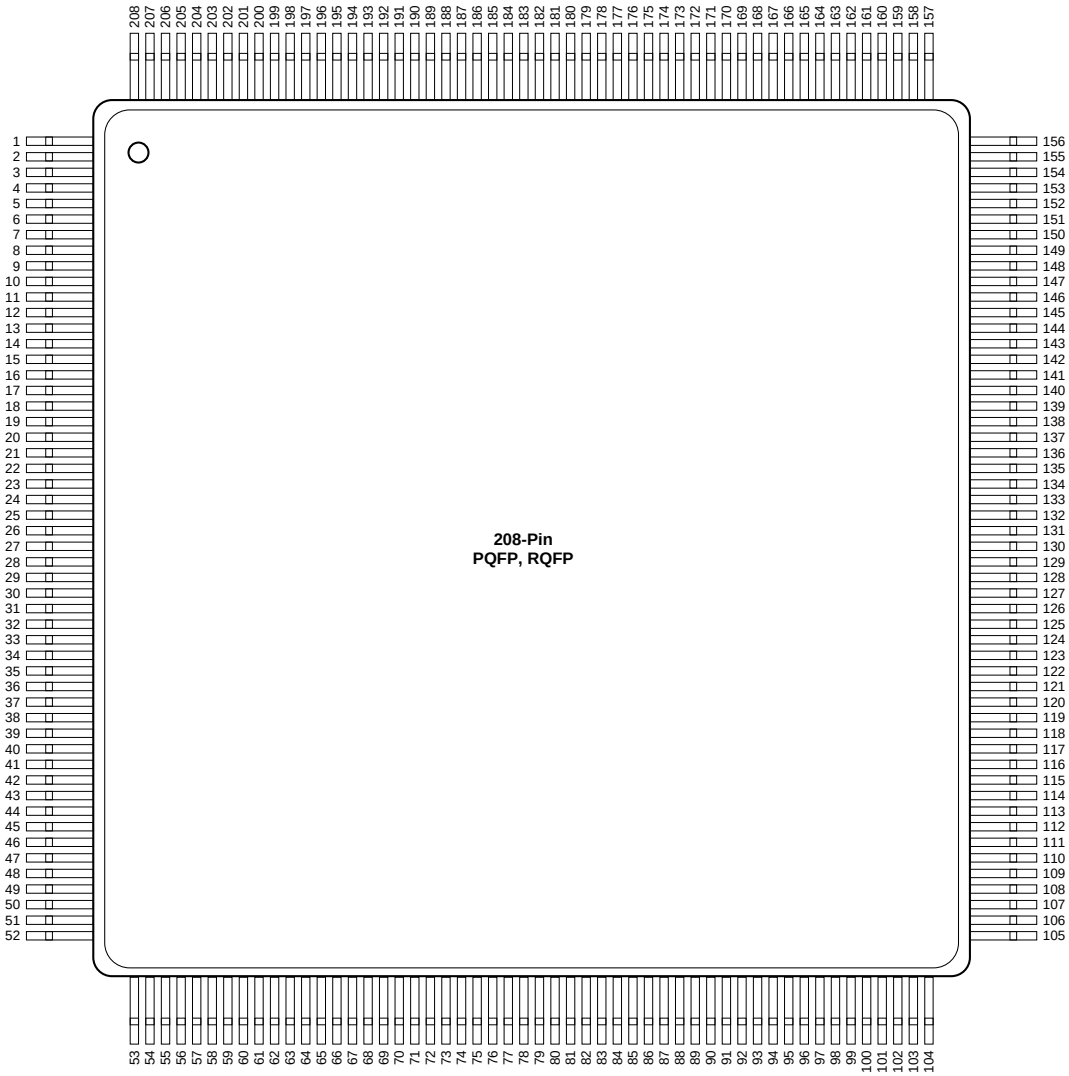
Pin Number	A1460BP Function
98	V_{CC}
99	V_{CC}
108	GND
109	V_{CC}
110	GND
119	I/O
121	I/O
122	V_{CC}
123	GND
124	V_{CC}
132	IOCLK, I/O
133	GND
138	I/O
152	CLKA, I/O
153	CLKB, I/O
154	V_{CC}
155	GND
156	V_{CC}
157	PRA, I/O
158	I/O
170	I/O
176	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC: Denotes "No Connection"*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

208-Pin PQFP, RQFP (Top View)



208-Pin PQFP, RQFP

Pin Number	A1460BP Function	A14100BP Function
1	GND	GND
2	SDI, I/O	SDI, I/O
11	MODE	MODE
12	V_{CC}	V_{CC}
25	V_{CC}	V_{CC}
26	GND	GND
27	V_{CC}	V_{CC}
28	GND	GND
40	V_{CC}	V_{CC}
41	V_{CC}	V_{CC}
52	GND	GND
53	NC	I/O
60	V_{CC}	V_{CC}
65	NC	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	V_{CC}	V_{CC}
79	GND	GND
80	V_{CC}	V_{CC}
82	HCLK, I/O	HCLK, I/O
98	V_{CC}	V_{CC}
102	NC	I/O
104	IOPCL, I/O	IOPCL, I/O
105	GND	GND
114	V_{CC}	V_{CC}

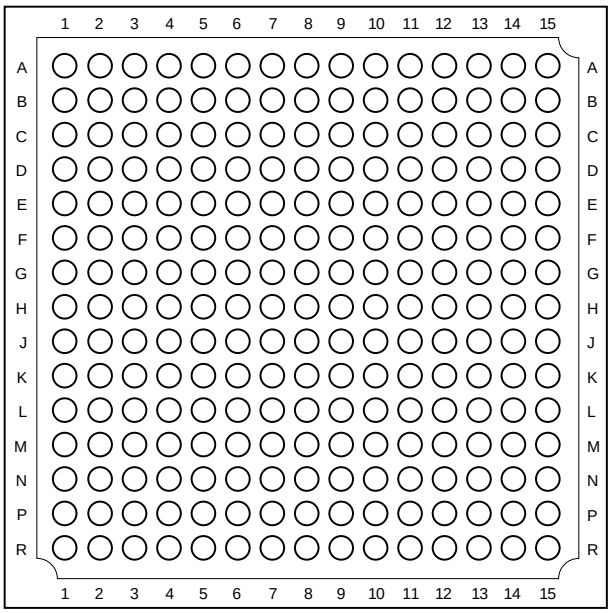
Pin Number	A1460BP Function	A14100BP Function
115	V_{CC}	V_{CC}
116	NC	I/O
129	GND	GND
130	V_{CC}	V_{CC}
131	GND	GND
132	V_{CC}	V_{CC}
145	V_{CC}	V_{CC}
146	GND	GND
147	NC	I/O
148	V_{CC}	V_{CC}
156	IOCLK, I/O	IOCLK, I/O
157	GND	GND
158	NC	I/O
164	V_{CC}	V_{CC}
180	CLKA, I/O	CLKA, I/O
181	CLKB, I/O	CLKB, I/O
182	V_{CC}	V_{CC}
183	GND	GND
184	V_{CC}	V_{CC}
185	GND	GND
186	PRA, I/O	PRA, I/O
195	NC	I/O
201	V_{CC}	V_{CC}
205	NC	I/O
208	DCLK, I/O	DCLK, I/O

Notes:

1. *All unlisted pin numbers are user I/Os.*
2. *NC: Denotes "No Connection"*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

225-Pin BGA (Top View)



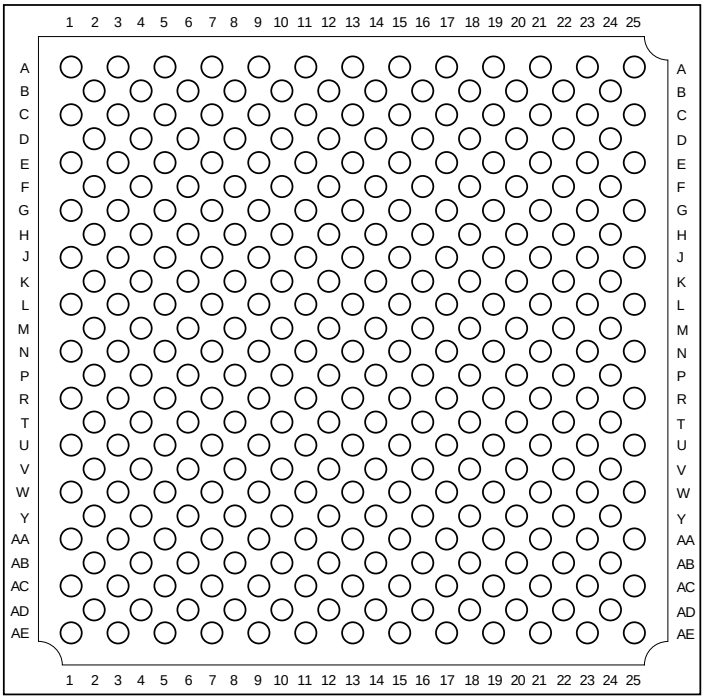
A1460BP Function	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA OR I/O	A7
PRB or I/O	L7
SDI or I/O	D4
V_{CC}	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

313-Pin BGA (Top View)



A14100BP Function	Location
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA OR I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
V_{CC}	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Take it to a higher level.

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